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PCIM MAGAZINE

Your power electronics magazine for industry news, hot topics and insights

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Editorial

Power electronics is developing rapidly and has now become a crucial factor in shaping a sustainable energy future. This dynamic is being driven by several key factors: the need to optimize energy consumption, the increased integration of renewable energies, and the growing demand for energy-efficient applications across various industries. In times of climate change and digitalization, the development of smart technologies is essential to creating a sustainable way of life.

Particularly in areas such as electromobility, smart buildings, and Industry 4.0, power electronics demonstrates its full potential. Advances in semiconductor technology, especially through innovative materials like silicon carbide (SiC) and gallium nitride (GaN), are enabling more efficient and compact solutions. One example is the 400 V SiC MOSFET, which is revolutionizing efficiency in applications ranging from electric vehicles to solar energy storage. Furthermore, the Fraunhofer Institute is highlighting the possibilities of new materials for high-frequency and high-power electronics with aluminum yttrium nitride (AlYN). Research in the field of power electronics is also setting new standards. The Leibniz University of Hanover, for example, is illustrating how gallium nitride (GaN) functions as a key technology in compact, high-performance supply solutions.

In this issue of the PCIM Magazine, we take a detailed look at these and other groundbreaking technologies and their practical applications. You can look forward to an exciting portfolio that ranges from new developments in battery management to the future of the digital twin concept and the crucial role of power electronics in sustainability.

In the PCIM Magazine, we offer you exciting insights into the world of power electronics. In each issue, we not only present the latest methods and systems, but also shed light on the backgrounds and perspectives of leading experts. You'll thus gain a comprehensive overview of the most important innovations and challenges that are shaping the future of our dynamic industry. Join us on the path to a sustainable and progressive tomorrow in power electronics and discover with us the possibilities of this groundbreaking technology!

Regards

Lisette Hausser

Vice President PCIM

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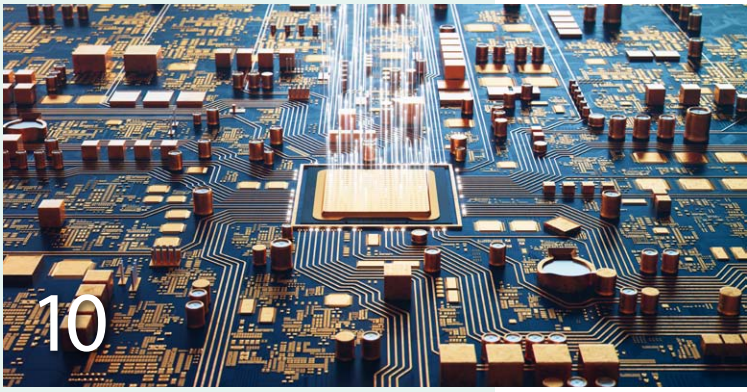


Job market for electrical engineers: no cause for concern

Corinne Schindlbeck, senior editor at WEKA Fachmedien

The job market is weakening, companies are undergoing transformation, AI is influencing job profiles, especially in the "White Collar" sector. Is the shortage of skilled workers over? We have compiled expert opinions. One thing is certain: the right skill set is becoming increasingly important, partly because of AI.

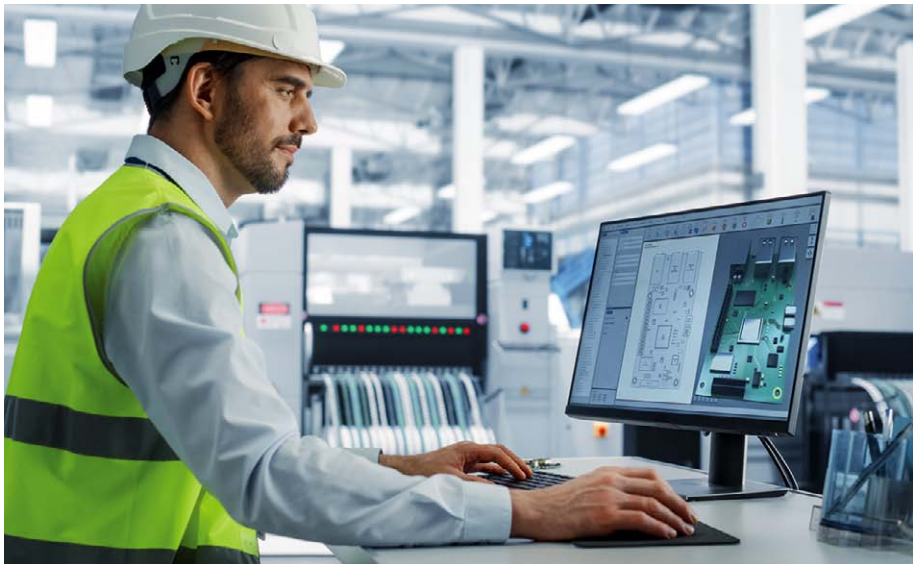


Image: Gorodenkoff/stock.adobe.com

As a Senior Economist at Indeed, Dr. Annina Hering regularly evaluates labour market data. The latest figures from Indeed show that vacancies for electrical engineers and software developers have fallen at an above-average rate, with electrical engineers even seeing a 20% drop compared to the previous year. This is a sharper decline than the German labor market average of -17 percent.

Hering notes that companies mainly save on high-paying, expensive positions. This also applies to software developers. But weren't they a rare and desperately sought-after resource not so long ago? Yes, but after the pandemic, companies have been hiring on a large scale with a kind of catch-up effect, explains Hering. In view of the lack of orders, companies are now questioning which positions are really strategically necessary. "Over-hiring" is currently being attempted to be corrected, which is also leading to job cuts in some places. At first glance, this may seem incomprehensible in view of demographic change – after all, a good three million baby boomers will retire in 2022 and a further 16.5 million will retire by 2036, according to a population forecast by the German Economic Institute – but it is "an observable trend", says Hering.

The recruitment consultancy Hays also has a good overview of the situation on the labor market thanks to regular analyses. Do electrical engineers need to worry about the decline in vacancies? No, says René Gruner. The job situation for electrical engineers is currently influenced by several factors.

Everything is being put to the test

Companies are currently more cautious when hiring new employees, as they have to pay more attention to costs due to a weakening economy. If the statements of the labor market institutes are to be believed, this attitude will continue in the coming months. Nevertheless, electrical engineers should not be discouraged. Despite the generally poor economic situation, some sectors are booming due to the energy transition and the pressure to invest more in electromobility. There are good job prospects here. In particular, the development and implementation of technologies for the use of renewable energies, the further development of electromobility and the digitalization of production processes offer concrete employment opportunities and job security for electrical engineers.

In difficult times like the current one, recruiting tends to be much more strategic, explains Nadja Eder, Managing Director of SchuhEder Consulting. People are becoming more aware of who they really need and who they don't, recruiters are "taking a more critical look again" and expectations are rising. "Job hopping", for example, i. e. changing employers in quick succession, is not welcome, a "stable career" is important, as are the right skills: flexibility, suitability and dealing with change management, a high affinity for IT and digitalization.

However, SchuhEder does not want to paint a gloomy picture of the engineering job market, quite the opposite. The vast majority of engineers have no problems. Even after redundancies, whether self-imposed or forced, they quickly find new employment. SchuhEder therefore describes the job market in the electronics industry as "extremely robust". Short-time work here and there and the

Dr. Annina Hering, Senior Economist at Indeed. She regularly evaluates labor market data.

current reluctance to hire new staff would not change this.

Junior positions in particular are in short supply, explains the consultant, "almost everyone is trying to attract young talent". However, companies also don't want to lose competent senior experts and, according to Eder, are in a good position if they have the right skill set. "Termination agreements in recent weeks and months have tended to affect people in their 60s without the desired qualifications and skills," explains the consultant.

While the focus shortly after Covid-19 was primarily on procurement and the supply chain, sales is now required to push the order situation in the difficult market environment. Sales engineers currently have good opportunities here.

René Gruner from Hays also sees opportunities. Yes, the recruitment requirements have indeed changed. In times of economic uncertainty, companies are placing greater emphasis on specific technical skills and soft skills, which are particularly relevant in the current situation. Knowledge in the areas of artificial intelligence, big data, cybersecurity and automation technology is particularly in demand.

In addition to technical skills, soft skills such as flexibility, problem-solving ability and, above all, the willingness to undergo continuous further training are becoming increasingly important. Companies are looking for candidates who not only have technical know-how, but are also able to adapt quickly to new challenges and develop innovative

INTERESTING TO KNOW

How much do you earn in power electronics?

SchuhEder Consulting is an official career partner of the PCIM and will be supporting the Career Area at the PCIM Expo next year. The team will be on site in person for discussions on Thursday, May 8, 2025. A panel discussion is also planned on the Technology Stage, which will focus on the latest developments in engineering salaries. To this end, SchuhEder Consulting is now collecting salary data that will be included in a report on the trade fair. Interested parties are invited to take part at www.schuh-eder.com/gehaltscheck/ and receive an individual evaluation and advice if required.

Would you rather be a doctor than an engineer?

Young people in Lower Saxony prefer to study human medicine and health sciences (up almost 28%) rather than engineering (down 7.7%). The number of prospective engineers at universities in Lower Saxony fell from around 53,000 in the 2014/15 winter semester to just under 49,000 recently – a drop of 8 percent. In mathematics and the natural sciences, the number fell from 24,000 to around 23,000 (minus 4 percent). In contrast, human medicine and health sciences experienced a boom (up 28% to more than 12,000 students) and the humanities also grew by 8% (to around 22,500 students).

Becoming AI-fit

In addition to traditional skills such as numerical and spatial thinking, technical understanding and electrophysical knowledge, engineers will also need to develop skills in dealing with AI applications in the future. For example, to make more precise forecasts for the utilization of energy grids, as Prof. Sebastian Lehnhoff, Professor of Energy Informatics at the University of Oldenburg, describes the use of AI in the smart grid in a recent VDE paper: "In IT, AI can be used in many fields of application for automation, optimization and decision support. These include the creation of precise forecasts for energy generation, consumption and market prices, predictive maintenance, automated algorithmic trading energy trading, grid management and control as well as applications in customer service and for product optimization."

Continuously new jobs (not only) around the energy transition

Are there specific areas/profiles in which the demand for electrical engineers is stable or even growing? There is, says René Gruner from the recruitment consultancy Hays: "The demand for professional profiles is growing, provided that candidates have relevant experience in the following areas:
Renewable energies
Electromobility
Industry 4.0.
Automation technology
Smart grids
Medical technology
IoT

sc

solutions. The ability to work in a team and strong communication skills are also important criteria, as many projects are carried out in interdisciplinary teams.

According to Gruner, another trend is the increasing importance of sustainability and environmental awareness. Companies are increasingly looking for engineers who have knowledge of sustainable technologies and processes and can contribute to achieving the company's ecological goals.

More choice

Companies that can afford to recruit anti-cyclically can currently hope to fill their vacancies as required. Like Inpotron, a manufacturer of power supply units and power supply solutions, whose balance sheet was hit by the sluggish economy this year for the first time in many years. With one advantage: all vacant positions have been filled "very well" and the supply of well-qualified personnel has increased, says Inpotron owner Hermann Püthe. The current period is therefore also an opportunity for recruiting, "if you can afford it and want it".

Incidentally, companies that can integrate English-speaking employees well have an advantage, as there are more English-speaking profiles on the market, especially in the technical areas, says Nadja Eder. However, many companies are not yet ready.

The influence of artificial intelligence

Sandra Maile is CEO at Fortec, supplier of individual components and systems in the fields of display technology, embedded systems

In difficult times like the current one, recruiting tends to be even more strategic, explains Nadja Eder, Managing Director of SchuhEder Consulting.

and power supplies. When staff turnover occurs, the company checks whether the vacant position can be developed further "through AI or the strategic direction of the company" and uses the opportunity to change things, she announced back in the summer. Does this mean that the substitutability of engineering work with AI is already playing a role?

Question to Dr. Annina Hering from Indeed. To a certain extent, she says. Recent studies by Indeed on AI have shown this. "We have investigated which skills generative artificial intelligence can take on today. And we can see that tasks involving mathematics and data in particular, as well as writing and reporting functions, can increasingly be performed by AI," says Hering. It will have an impact on job profiles if AI agents increasingly take on routine tasks. Engineers would concentrate on their core tasks.

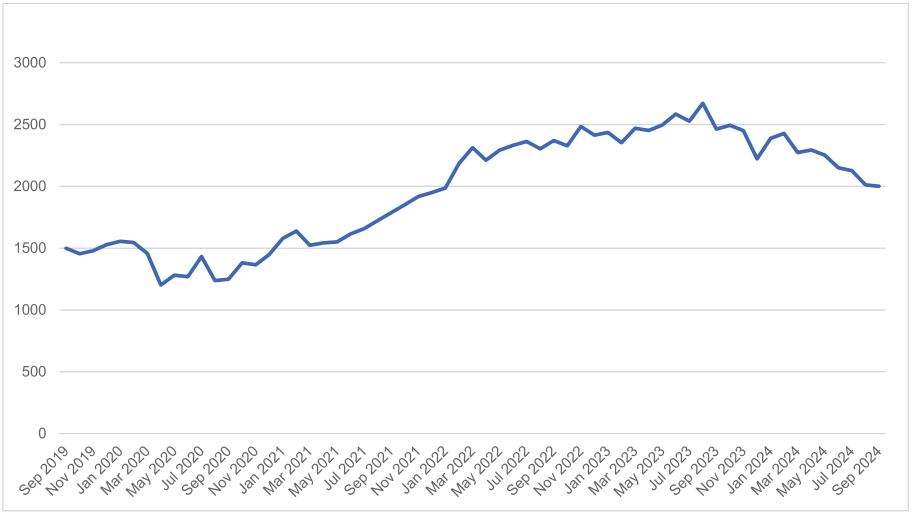
Nevertheless, AI will probably only slightly alleviate the shortage of engineers at best. The experts currently seem to agree on this. For example, Dr. Britta Matthes from the Institute for Employment Research (IAB), who analysed the substitutability of engineers for a VDE paper. "High substitutability potential does not mean that the professions will no longer exist in the future." Rather, the aim is to make the work of engineers more efficient and free up time for more complex, creative tasks through automation. Matthes therefore gives the all-clear to those who are worried about AI: The use of AI requires the assessment and classification of engineers, their knowledge. AI can only be used productively when it is combined with specialist knowledge.

Matthes therefore does not believe that the demand for engineers in electrical engineering and information technology will decrease in view of the great potential for automation in engineering work. Instead, she even anticipates a "significant increase in demand". This is because the combination of demographic change, which will see many engineers retire, and increasing digitalization will lead to growing demand.

However, this also means that the "skill set" for personal employability is becoming increasingly important – a hobbyhorse of Prof. Thorsten Weiss from Ravensburg-Weingarten University of Applied Sciences (RWU). Especially in view of the currently weakening job market. A degree alone is no longer enough to get your dream job effortlessly. "In my observation, generalists no longer have it so easy. Employers are currently looking specifically for suitable candidates for their specific tasks, as familiarization with complex topics is very time-consuming and expensive."

Engineers can also take confidence from the non-cyclical factors. The slump does not change the structural shortage of skilled workers. The Bavarian Industry Association (vbw) is reporting insolvencies, short-time working and declining employment (and is therefore warning the negotiating partners against overambitious wage demands). However, measures to secure skilled workers are just as urgent. This is because the shortage of skilled workers and labor will remain a challenge in the medium and long term. The reason: an ageing society. mk

Image: Indeed



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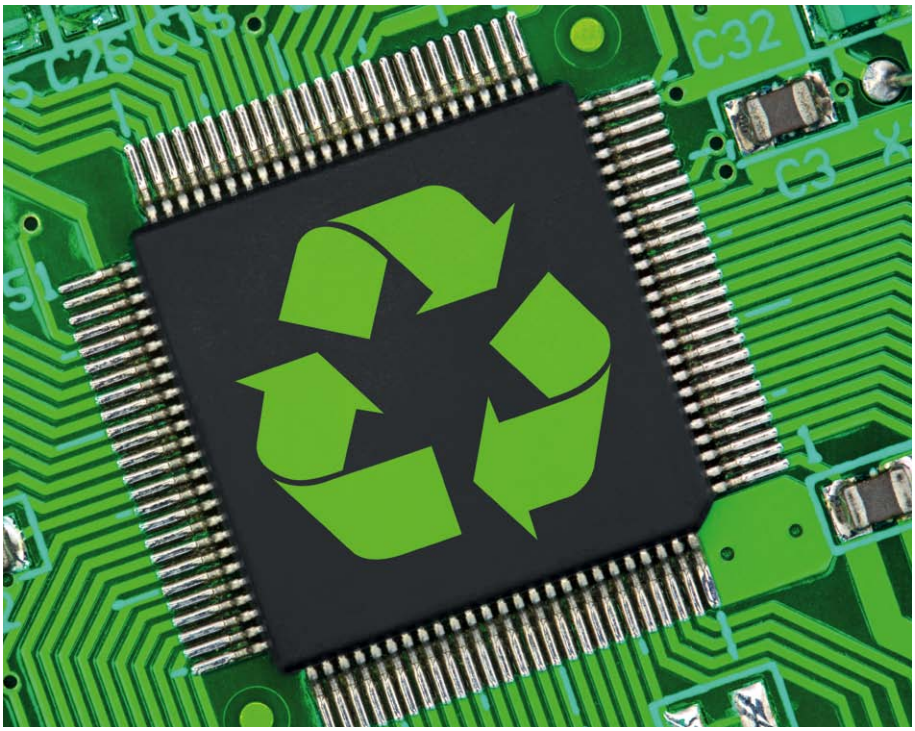
"The semiconductor industry is very skeptical about recycling of semis"

An interview with Ole Gerkensmeyer, Vice President EMEA Sales at Nexperia. By Engelbert Hopf, senior editor at WEKA Fachmedien

The amount of electronic waste is increasing worldwide year on year. With the imminent transition to an all-electric society, the amount is likely to increase even further. We spoke to Ole Gerkensmeyer, Nexperia, about the opportunities for the semiconductor industry to move towards a circular economy.



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Without comprehensive electrification and digitalisation, it will hardly be possible to achieve the goal of an all-electric society. Conversely, what does this mean for electronic waste?

The UNTAR "e-waste monitor 2024" records e-waste as the fasted waste stream globally with a growing trend, and so does the EU by the way, based on data for the year 2022. Besides the UN we have consensus across larger economic expert groups like McKinsey and others, that cloud computing and AI, transportation in all forms, the electrification of many industries like steel and construction, as well as the need to respond to the consequences of global warming, desalination and more air conditioning will require an even faster growth of electronic demand – and unfortunately, e-waste.

Can you give us an idea of the current dimension of electronic waste? To what extent has it increased in recent years?

The UNITAR report lists 62 m tons of e-waste for 2022. Growth is here.

Are there any estimates as to how big the problem could become in the future if things continue as they are? Are there also committed scenarios for the future?

Short answer: UNITAR see 4 scenarios: normal, progressive, ambitious and aspirational with growing amount of waste but also growing amount of biz potential, but: The graphic suggests that the higher the purchasing power of a country, the higher contribution to e-waste. As a scenario moving forward: as we aim to reduce world hunger and poverty one of the consequences likely is an exponential increase in e-waste.

Committed scenarios: well, in the EU we have now the right to repair since 2024, which is a start but nowhere close to the necessities for reducing e-waste beyond recycling. The EU recommends circular economy and "highest possible re-use" but so far I have not yet met a single electronic company who does that.

Electronic waste ranges from large appliances, such as those used in medical technology, to electronic toys. Which of these categories contributes most to the growth of electronic waste?

Please note that transportation with electric cars is NOT YET a category!

The buzzwords that are repeatedly mentioned in this context include recycling and urban mining. What significance do recycling and urban mining have for the supply of raw materials in the electronics industry today?

They could supply a growing percentage of raw material needs. However, with re-use beyond re-cycling that need would be more meaningful.

- We have unnecessary global e-waste movements to other countries.
- Urban mining as recovery of metals from e-waste is at low percentages.
- Urban mining does represent a massive revenue potential, currently not considered, which is exceeding 30 – 50 B USD, depending on the scenario.

If we break the whole thing down to power semiconductors, what significance has recycling had for this sector so far, and what significance could it take on in the future?

The semiconductor industry is very skeptical about recycling of semis given that any known processes are rather destructive to the

Ole Gerkensmeyer, Nexperia:
"Electronic waste is not just a problem in underdeveloped countries, in the EU we recycle 42 percent, but that means the 58 percent of e-waste are rotting in undetermined state – I'm not sure our grandchildren will be happy with today's ignorance."

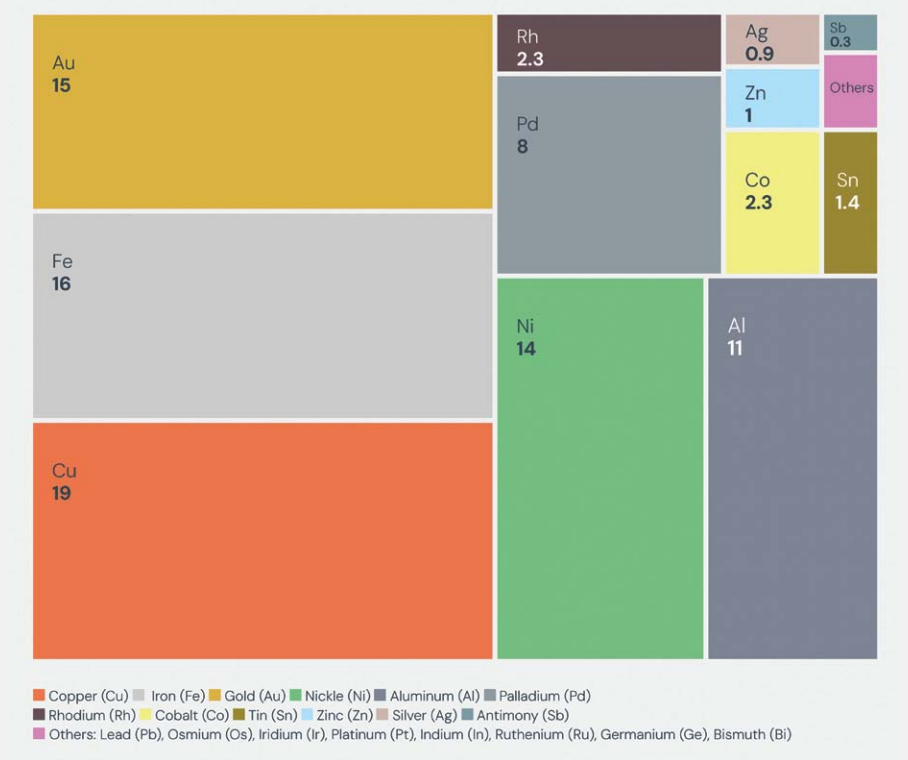


Image: The Global E-waste Monitor 2024

In 2022, the overall gross value of the metals contained in e-waste was estimated at USD 91 billion. Most of the potential value in secondary raw materials in e-waste lies in copper (USD 19 billion), iron (USD 16 billion) and gold (USD 15 billion).

devices. As such "recycling" of semis is little to not meaningful.

When it comes to recycling, it's always about the quality of the recycled materials. Is this generally sufficient for reuse, or are there only a few material areas in which recycled materials could be used again in the electronics industry?

Recycling in electronics typically describes as what is written in the "WEEE" guidelines, basically the disassembly into ingredients without electronic function. So, in short: re-use would only be possible "prior" to recycling, id est through modular application design with modular electronic systems which can be exchanged.

Does the recycling of materials in the electronics industry currently make economic sense at all, or are the prices on the global market at a level that would make the use of recycled materials economically unattractive?

Recycling does make sense, and as UNITAR has pointed out there is a massive potential still through higher recycling rates and urban mining, 30 – 50 billion dollars a year. However, "just" looking at recycling would ignore the fact that many electronic boards and systems are fully functional when they are recycled, as such we – as society – throw away fully functional products – that does NOT seem to be smart.

How high is the share of European, Asian and American industrialised countries in the 'production' of electronic waste? Do these countries have politically defined targets regarding the collection and recycling of electronic waste?

Europe is leading the pack with 17.6 kg/capita e-waste. Outside Europe we have a growing number of countries, starting to define targets for e-waste reduction and increased recycling rates.

The public consciousness often associates electronic waste with electronic waste dumps in Africa. How big is the problem of illegally disposed electronic waste, which can then hardly be recycled effectively in developing and newly industrialising countries?

I think, we as society do NOT GRASP the size of the problem yet. As per above, we release several tons of very toxic materials into the earth, polluting drinking water, causing trees and plants to die, then animals and then us. It is not just a problem in underdeveloped countries, in the EU we recycle 42 percent, but that means the 58 percent of e-waste are rotting in undetermined state – I'm not sure our grandchildren will be happy with today's ignorance.

Would repair and refurbishment be a complementary way in the electronics industry to avoid further increasing electronic waste? How much progress has been made on these issues so far?

Little to none: in the year 2024, the EU created the law for "right to repair" but this is just starting, try to repair your electric car, your washing machine, coffee machine, mobile phone,…

What contribution could component manufacturers make to reducing the constant increase in electronic waste? Aim for higher levels of integration, promote the use of module solutions?

In my view all involved parties can provide:

- information on the durability of the products
- tools how to measure durability/health over operating life time
- strongly promote modular usage with options for exchange/swap/upgrade – and circular business cases where to use the swapped/exchanged old modules
- upstream education through the supply chain, pointing out "throw-away" design mentality and suggest/recommend more sustainable options

The questions were asked by E. Hopf. mk

AlYN promises more energy-efficient and powerful electronics

Engelbert Hopf, senior editor at WEKA Fachmedien, based on documents from the Freiburg Fraunhofer Institute IAF

This summer, researchers at the Fraunhofer Institute IAF succeeded in producing and characterising a promising new semiconductor material, aluminium yttrium nitride (AlYN), using the MOCVD process. AlYN has enormous potential for use in energy-efficient high-frequency and high-performance electronics.

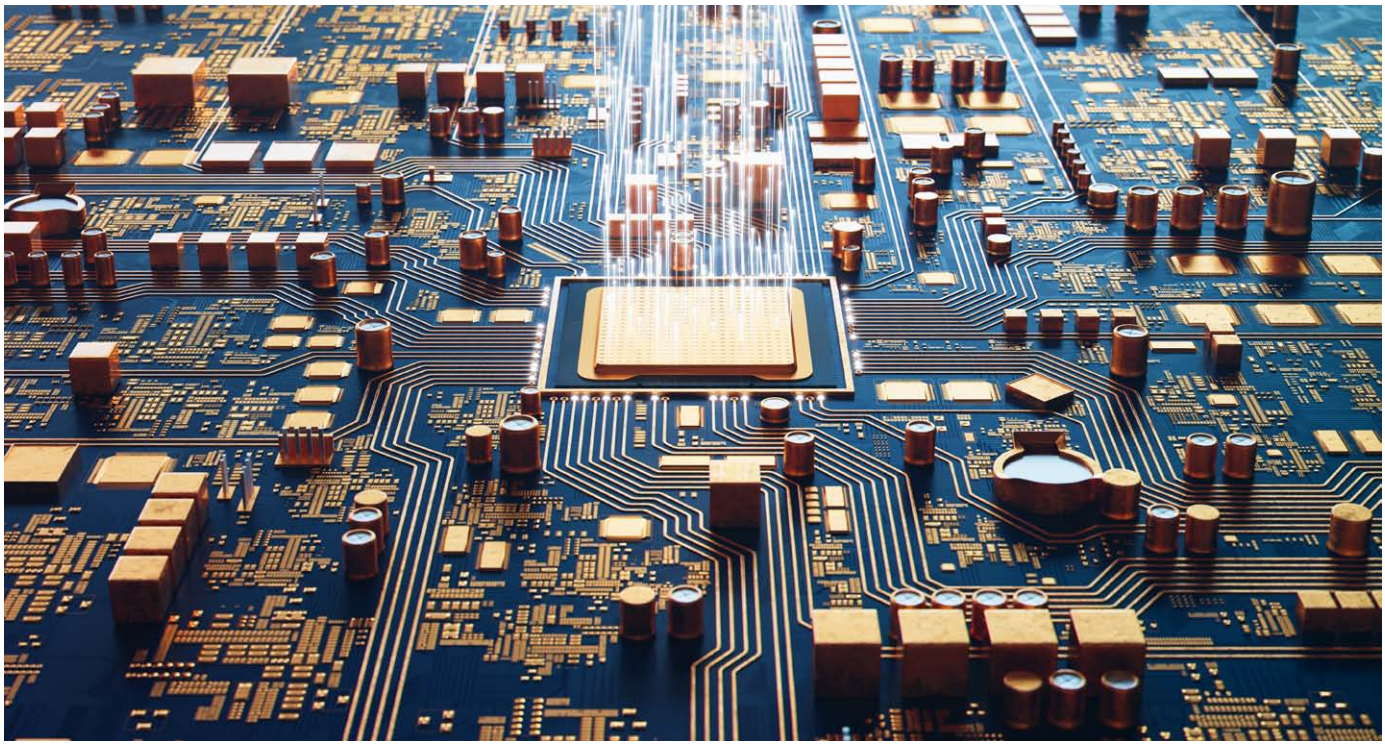


Image: Dabarti/stock.adobe.com

Due to its outstanding material properties, aluminium yttrium nitride had already attracted the interest of various research groups in the past. However, the growth of the material has so far presented a major challenge. So far, it has only been possible to deposit AlYN using the magnetron sputtering process. Researchers at the Fraunhofer Institute for Applied Solid State Physics IAF have now recently succeeded in producing the new material using MOCVD technology (metal-organic chemical vapour deposition), thus enabling the development of new, diverse applications.

"Our research marks a milestone in the development of new semiconductor structures. AlYN is a material that enables an increase in performance while minimising energy consumption and can thus pave the way for innovations in electronics that our digitally networked society and the ever-increasing demands on technologies urgently need," says Dr. Stefano Leone, scientist at Fraunhofer IAF in the Epitaxy department. Due to its promising material properties, AlYN can become a key material for future technological innovations.

From the aluminium yttrium nitride layer to heterostructure

Recent research had already demonstrated the material properties of AlYN, such as ferroelectricity. When developing the new compound semiconductor, the researchers at Fraunhofer IAF focussed primarily on its adaptability to gallium nitride (GaN). The lattice structure of AlYN can be optimally adapted to GAN and the AlYN/GaN heterostructure promises significant advantages for the development of future-oriented electronics.

Last year, the research group at Fraunhofer IAF had already achieved groundbreaking results when they succeeded for the first time in depositing a 600 nm thick AlYN layer. This layer with a wurtzite structure contained an unprecedented yttrium concentration of over 30 per cent. A further breakthrough

Image: Fraunhofer IAF

The different colour nuances of the AlYN/GaN wafers visible here result from different yttrium concentrations and growth conditions.

was recently achieved: It has been possible to produce AlYN/GaN heterostructures with precisely adjustable yttrium concentration, which are characterised by excellent structural quality and electrical properties. The new heterostructures have a yttrium concentration of up to 16 per cent. Under the leadership of Dr. Lutz Kirste, the structural analysis group carried out further detailed analyses to deepen the understanding of the structural and chemical properties of AlYN.

In addition, the Fraunhofer researchers have already been able to measure very promising electrical properties of AlYN that are interesting for use in electronic components. "We were able to observe impressive values for sheet resistance, electron density and electron mobility. These results have shown us the potential of AlYN for high-frequency and high-performance electronics," says Dr. Leone.

AlYN/GaN for high-frequency applications

Thanks to its wurtzite crystal structure, AlYN can be adapted very well to the wurtzite structure of gallium nitride with a suitable composition. An AlYN/GaN heterostructure promises the development of semiconductor devices with improved performance and reliability. In addition, AlYN has the ability to induce a two-dimensional electron gas (2DEG) in heterostructures at a yttrium concentration of about 8 per cent.

From the results of the material characterisation, it can be deduced that AlYN can be used in transistors with high electron mobility (HEMTs). The researchers were able to observe a significant increase in electron mobility at low temperatures (more than 3000 cm^2/Vs at 7 K). Meanwhile, the team has already made significant progress in demonstrating the epitaxial heterostructure required for fabrication and is continuing to explore the new semiconductor with a view to producing HEMTs.

The researchers in Freiburg can also already venture a positive prognosis for industrial use: with AlYN/GaN heterostructures grown on 4-inch SiC substrates, they were able to demonstrate the scalability and structural uniformity of the heterostructures. The successful production of AlYN layers in a commercial MOCVD reactor enables scaling up to larger substrates in larger MOCVD reactors. This method is considered to be the most productive for the production of large-area semiconductor structures and emphasises the potential of AlYN for the large-scale production of semiconductor components.

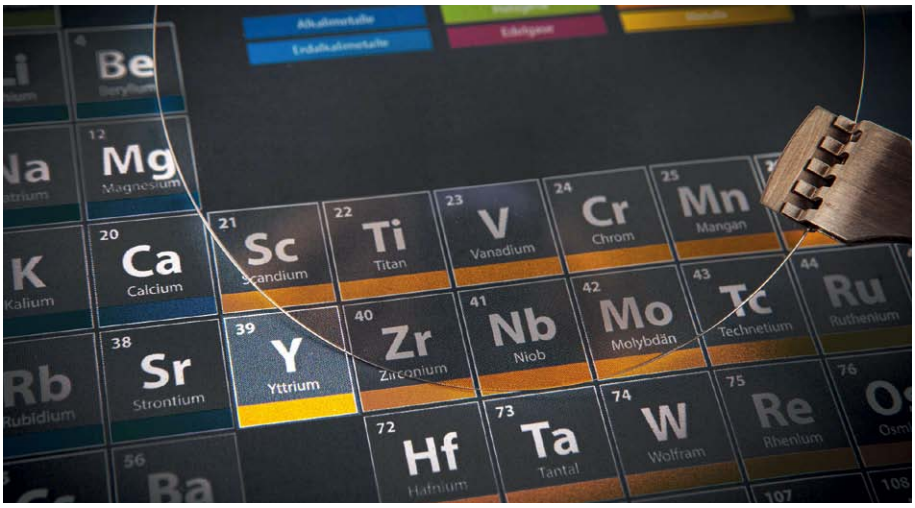


Image: Fraunhofer IAF

Researchers at Fraunhofer IAF in Freiburg have succeeded in growing AlYN/GaN heterostructures in a MOCVD reactor on 4-inch SiC substrates.

Development of non-volatile memories

Due to its ferroelectric properties, AlYN is highly suitable for the development of non-volatile memory applications. Another important advantage is that the material does not have a layer thickness limit. Therefore, the research team at Fraunhofer IAF encourages further research into the properties of AlYN layers for non-volatile memories, as AlYN-based memories can drive sustainable and energy-efficient data storage solutions. This is particularly relevant for data centres, which are used to cope with the exponential increase in computing capacity for artificial intelligence and have significantly higher energy consumption.

Oxidation as a challenge

A major hurdle for the industrial use of AYN is its susceptibility to oxidation, which impairs the material's suitability for certain electronic applications. "In the future, it will be important to research strategies to minimise or overcome oxidation. The development of high-purity precursors, the application of protective coatings or innovative manufacturing techniques could contribute to this. So far, the susceptibility of AlYN to oxidation has been a major challenge for research to ensure that research efforts are focused on the areas with the greatest chance of success," Dr. Leone therefore demands. eg

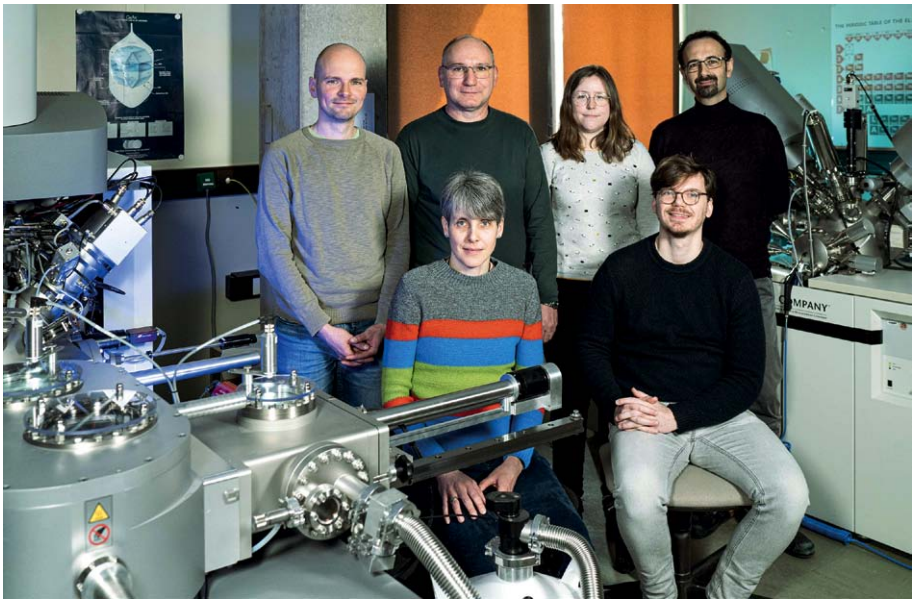


Image: Fraunhofer IAF

With their work on epitaxy and characterisation of AlYN/GaN heterostructures, the Fraunhofer IAF research team has achieved a breakthrough in the field of semiconductor materials.

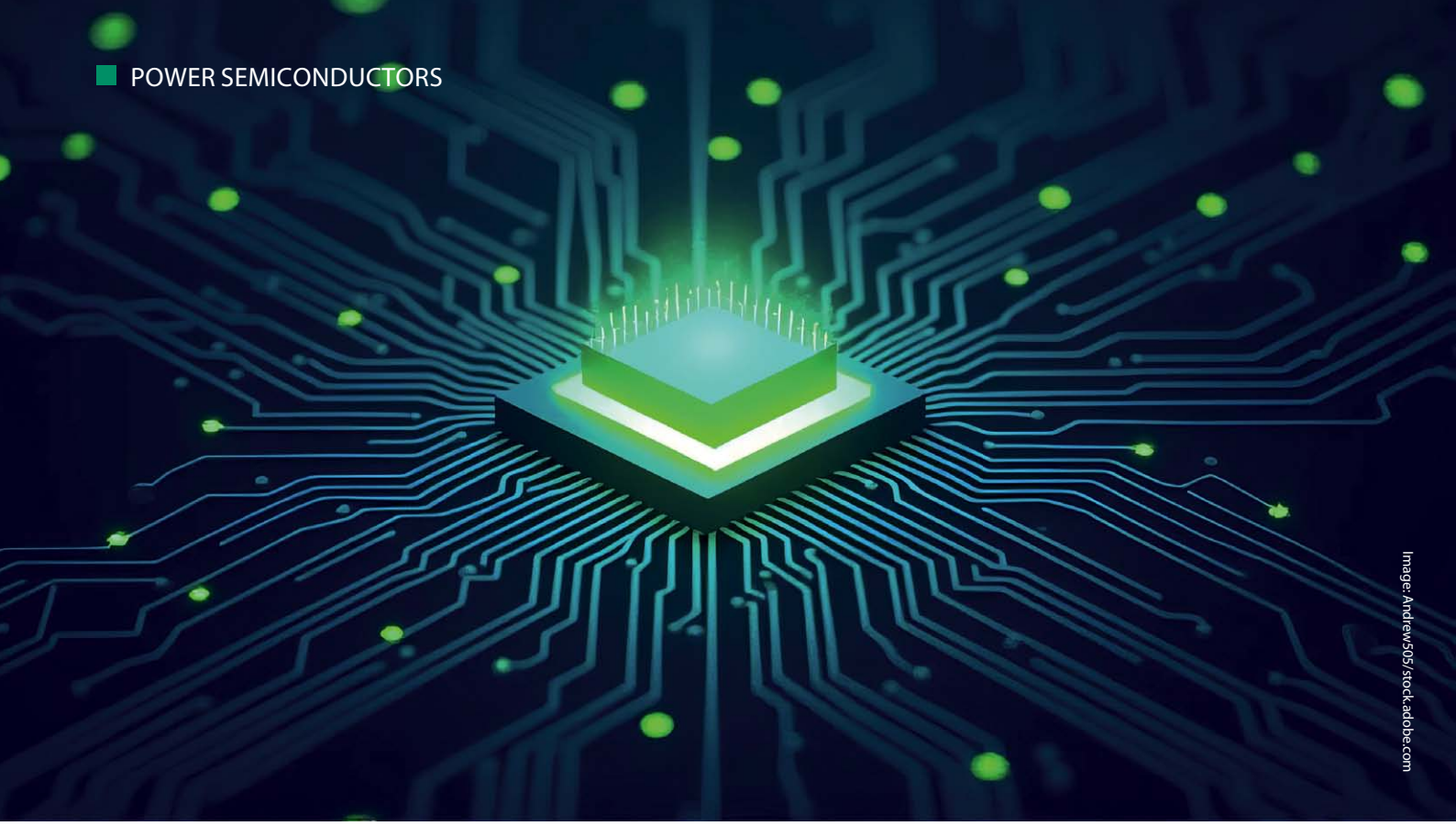


Image: Andrew505/stock.adobe.com

Unlocking new efficiency and power density possibilities with CoolSiC MOSFETs 400 V G2

Dr. Martin Wattenberg is responsible as a System Application Engineer for the development of innovative systems using WBG switches. Sriram Jagannath, M. Sc., works as a Staff Engineer in Product Definition and Application Engineering and is responsible for the CoolSiC MOSFET 400 V G2 portfolio. Dr. Ralf Siemieniec is a Senior Principal Engineer and works on the development of technology concepts for silicon and silicon carbide MOSFETs.

Infineon's CoolSiC MOSFETs 400 V G2 are designed to bridge the gap between 200 V Si trench MOSFETs and 650 V SiC trench MOSFETs, to address two-level topologies for bus-voltages up to 300 V (DC) and enabling the adoption of innovative three-level topologies for bus voltages up to 600 V (DC). These cutting-edge devices offer ultra-low switching losses and low on-state resistance ($R_{DS(on)}$), making them ideal for a wide range of applications like AI server and datacenter power supplies, solar and energy storage systems, uninterruptible power supply, motor control, Class-D audio amplifiers, among many others.

Optimized for 2-level topologies with 120 V (AC) input voltage or up to 300 V (DC) input voltage, and 3-level topologies with 230 to 350 V (AC) or 400 to 600 V (DC) input voltages, CoolSiC MOSFETs 400 V G2 deliver significant gains in switching figures-of-merit (FoMs) and $R_{DS(on)}$ stability over junction temperature. This makes them a perfect fit for hard-switching applications, such as bridgeless bidirectional CCM totem pole PFCs (Figure 1), and soft-switching applications, like synchronous rectifiers, to achieve the highest possible system efficiency and power density while optimizing the performance-to-cost ratio.

This article delves into the technology behind CoolSiC MOSFETs 400 V G2 and verify the expected efficiencies and power density gains through measurements in a 3-level flying capacitor CCM (continuous conduction mode) totem-pole PFC (power factor correction) technology demonstrator. By comparing the results with those of a common 2-level totem-pole PFC using 650 V SiC MOSFETs, we showcase the benefits of this innovative technology and its potential to transform the industry.

New 400 V SiC trench MOSFET structure for improved performance

Building on the success of first-generation CoolSiC devices, the new 400 V SiC MOSFET takes advantage of continuous technology

advancements to deliver even better performance. By reducing the cell pitch and refining channel properties, significant improvements in device performance have been achieved. Moreover, an enhanced control over drift region properties enables more precise management of the device's behavior. Through meticulous optimization of the chip design, for example the junction termination, the active area loss has been minimized. The result is a next-generation 400 V SiC MOSFET that sets a new standard for performance, reliability, and efficiency, enabling the development of more innovative and sustainable power electronic systems.

By combining the CoolSiC 400 V with a low-inductance package like TO-Leadless (TOLL), designers can create optimized PCB (printed circuit board) layouts that fully leverage the device's exceptional switching performance. The high C_{oss} linearity and commutation-robust body diode with low Q_{rr} work together to minimize V_{DS} overshoots and ringing, ensuring stable switching waveforms that are virtually independent of operating temperature and load current. The excellent switching FoMs translate to high switching speeds resulting in minimized switching and dead-time losses, which result in improvement in efficiency and power density with good EMI (electromagnetic interference) performance.

Putting CoolSiC 400 V to the test: Performance evaluation in a totem-pole Power Factor Correction

The bridgeless 2-level (2L) totem-pole PFC topology is the state-of-the-art solution for high-efficiency and high power-density designs, eliminating diode-related losses and offering good performance, with efficiencies reaching up to 99 percent. This versatile topology can be operated in various control modes, including continuous current mode (CCM), discontinuous current mode (DCM), critical current mode (CrCM), and triangular current mode (TCM), and is inherently capable of bidirectional power flow. However, to take efficiency and power density to the next level in systems with input voltages ranging from 180 to 350 V (AC), multi-level topologies are the way forward. One promising approach to further boost power density is the 3-level (3L) flying capacitor CCM totem-pole topology, as illustrated in Figure 1.

By connecting two devices in series in the high-frequency (HF) leg, for the same DC output voltage, the blocking voltage requirement for each device is halved, resulting in significantly reduced switching losses. Additionally, the voltage swing across the inductor is also halved. When combined with the benefits of "series interleaving" inherent to the flying capacitor topology, the effective switching frequency is doubled compared to the device switching frequency. The higher effective switching frequency combined with a lower voltage swing across the inductor allows for a significant reduction (1/4) in the boost inductance at the same current ripple. For high power rated converters ≥3 kW, the CCM mode of operation in 3L flying capacitor topology enables lower switching losses, lower RMS current related conduction losses, and easier control and EMI filter design due to fixed frequency operation. The combination with an interleaved approach opens the door to an even higher power density.

The challenges with the design of 3L flying capacitor topology include – startup, pre-charging and balancing of the flying capacitor under different operation conditions and implementing a robust gate-drive for the floating HF leg MOSFETs. These challenges have been addressed in an upcoming 3.3 kW 3L-flying capacitor PFC reference design from Infineon but have also been investigated widely in the literature due to the significant benefits offered by the topology. Infineon is also positioning the system-solution as a cost-competitive high-performance alternative to the traditional 2-level-CCM totem pole topology for the highest efficiency and power density in the AC/DC PFC stage.

A technology demonstrator for the 3L flying capacitor topology, capable of up to 5.6 kW, was built and is shown in Figure 3. Two interleaved 3-level flying capacitor boost PFC legs are seen in the front. The empty area in the back is reserved for an LLC DC/DC converter for down-conversion to 48 V. With each individual MOSFET in HF PFC leg switching at 80 kHz, the effective switching frequency of a single 3L boost stage is 160 kHz. To further raise the effective frequency seen by the EMI filter, a second interleaved stage is used for an effective frequency of 320 kHz. A hold-up extension circuit (not shown) allows the utilization of more energy out of the DC-link, thus reducing its size. The inductor with an inductance of 50 µH is realized with a RM12LP ferrite core and optimized using litz wire. The power stage uses 400 V, 45 mΩ IMT40R045M2H SiC MOSFETs. Switching frequency and inducto size can

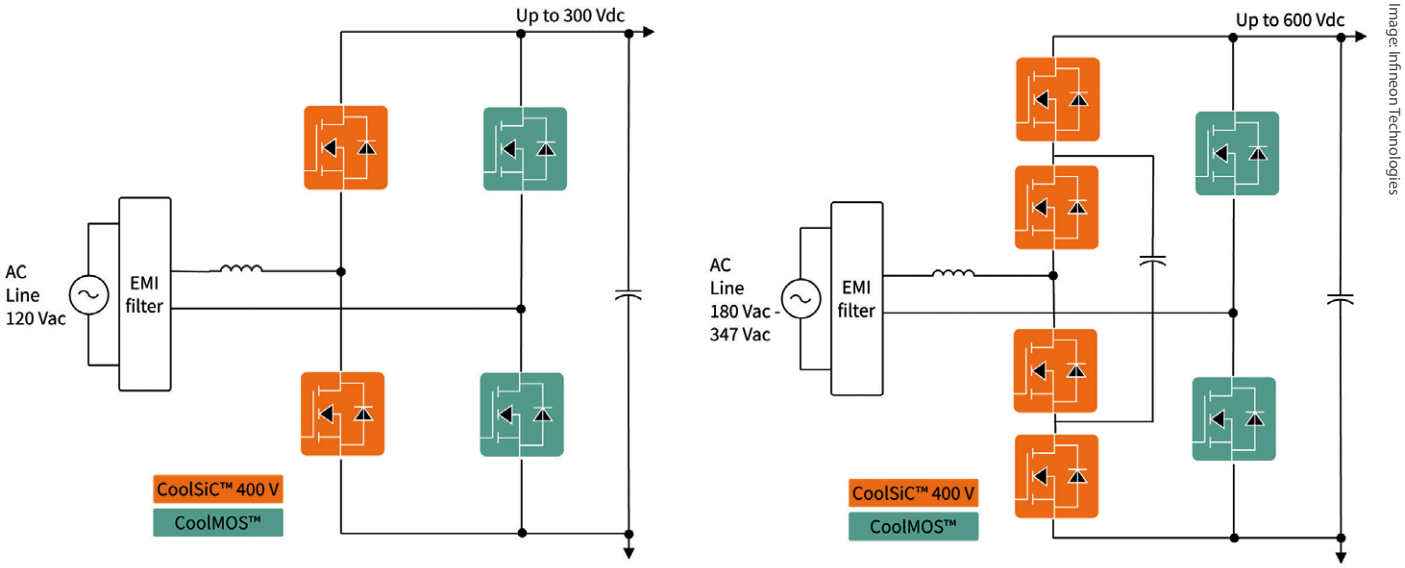


Image: Infineon Technologies

Figure 1: Application examples for CoolSiC 400 V: two-level and three-level bidirectional totem-pole topology, depending on the AC voltage.

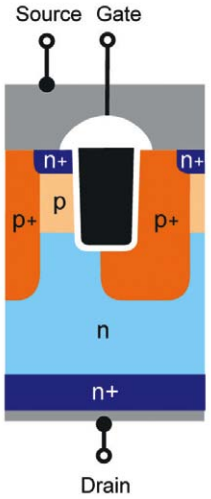
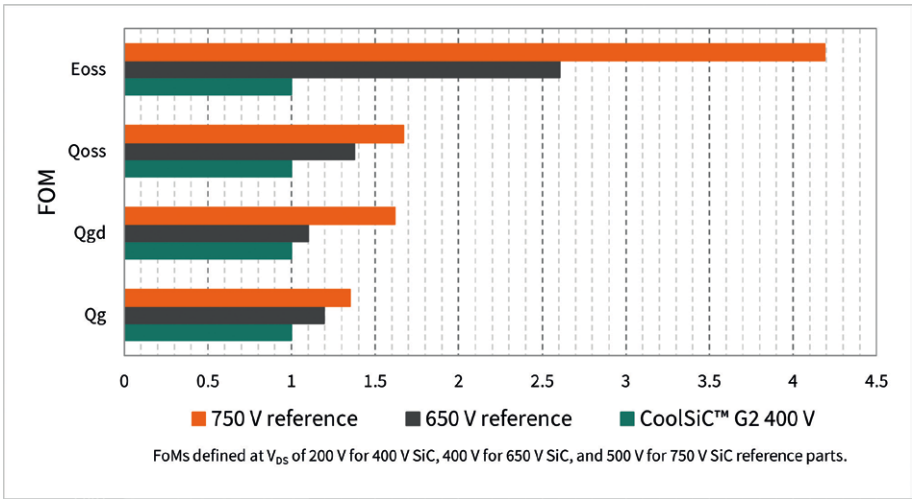


Figure 2: CoolSiC 400 V G2 trench MOSFET structure resulting in improved switching FoMs and stable $R_{DS(on)}$ dependence on junction temperature.



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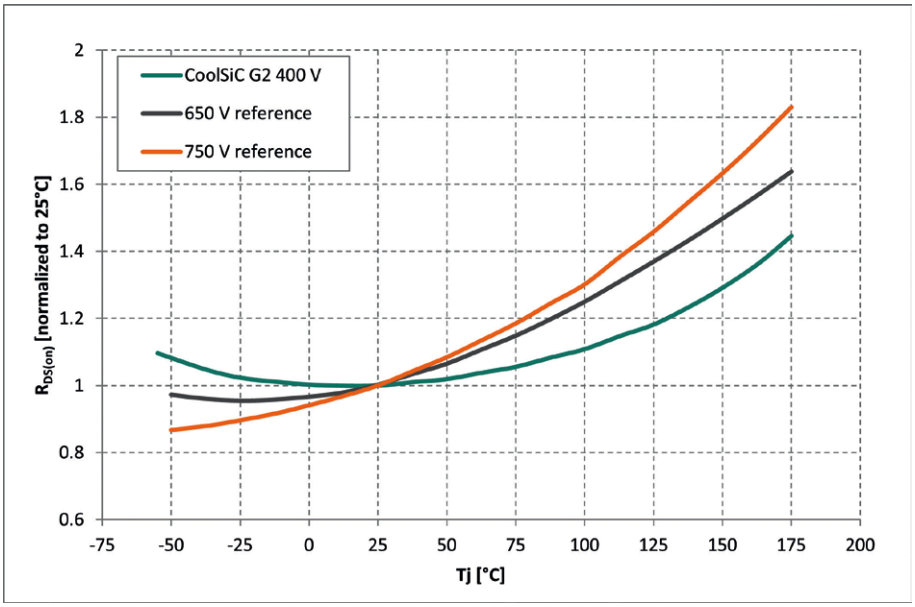


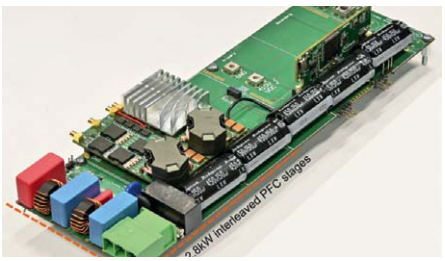
be further tuned for higher peak-efficiency or power-density, e. g. by operating the full system well above 400 kHz (>100 kHz per device).

The results presented here use only one of the two interleaved boost stages to facilitate a comparison with the common 2L 3.3 kW totem-pole (TP) PFC that uses 650 V SiC trench MOSFET, as well as with a Classic or Dual Boost PFC employing SJ devices. For the efficiency comparison presented in Figure 4, the 3L FC TP PFC uses CoolSiC MOSFETs 400 V G2, 2L TP PFC uses CoolSiC MOSFETs 650 V G2, while the Dual Boost PFC uses CoolMOS P7, and the Classic Boost PFC uses CoolMOS CFD7A devices. The 3L FC TP PFC outperforms the 2L TP PFC at an AC input voltage of 230 V while operating close to 2.5x the switching frequency. The difference in efficiency at 2.5 kW is substantial: 99.15 percent vs. 98.9 percent, which translates to over 25 percent fewer losses in power conversion. This means significantly lower cooling efforts, making it an attractive solution for data centers and other applications where energy efficiency is key. What's more, the peak efficiency improves from 99.19 percent for the 2L TP PFC to 99.35 percent with the 3L FC TP PFC.

With the series connection of two 400 V devices, giving a theoretical blocking voltage of 800 V, even higher voltages can be addressed easily. Especially considering the increased power demand of AI in data centers, AC input voltage levels of 277 V (AC) or even up to 350 V (AC) are under evaluation. As can be seen from Figure 4, an increase in the AC input voltage level is also beneficial for the efficiency. In case of 265 V (AC), the peak efficiency further increases to a peak value of nearly 99.5 percent and full load efficiency of 99.35 percent.

Conclusions and outlook

The latest CoolSiC MOSFETs 400 V G2 from Infineon offer lower on-state resistances and better Figures-of-Merit over existing solutions, and benefit from a flat temperature



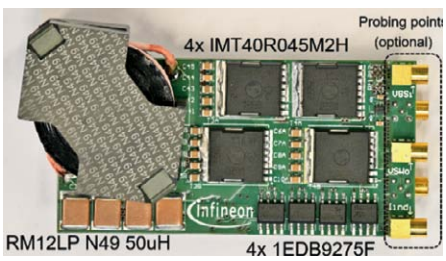


Image: Infineon Technologies

Figure 3: Technology demonstrator platform: Physical PSU mainboard (270 x 83 mm², 22 mm height) with 2x interleaved 3-level flying capacitor HF legs for PFC, which are 32 x 60 mm² in size.

dependence of the on-resistance. Low gate-, gate-drain, output- and reverse-recovery charges provide a highly controllable fast-switching capability.

The device performance has been investigated in an ultra-high power density PFC targeting next generation AI server and telecom power supplies. The measurements reveal that the device behaves well even at high switching speeds of 100 V/ns and above. The losses in the investigated PFC design are well-balanced across the different components. The achieved efficiency reaches close to 99.5 percent, with a calculated power density of 140 W/in³. Such power supply units pave the way to next generation AI server and industrial switched-mode power supplies (SMPS), capable of offering scalable solutions to deliver an output power of 5.5 to 8 kW and beyond.

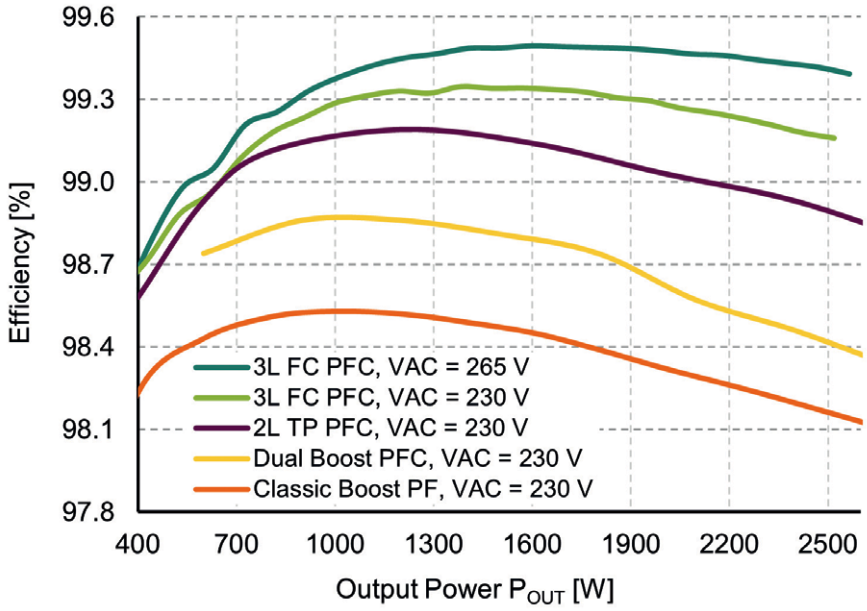


Image: Infineon Technologies

Figure 4: Efficiency comparison between the 3L FC TP PFC using 400 V SiC MOSFETs, a 2L TP PFC using 650 V SiC MOSFETs and a classic and dual boost PFC employing 650 V SJ MOSFETs (with applied line filter in the power analyzer).

Other application fields enabled by these new 400 V devices include solar and motor-control inverters employing a 3L ANPC inverter topology, or battery-connected drives for light electric vehicles, which could benefit from a higher battery input voltage of 288 V (achieved by a serial instead of parallel connection) using a simple B6 topology, MPPT buck-boost stage of a PV inverter, Class-D audio amplifiers, among many others. eg

The goal: a 200 W power supply based on GaN

Iris Stroh, senior editor at WEKA Fachmedien

At this year's ISSCC, the team of developers led by Professor Bernhard Wicht of Leibniz University Hanover presented a fully integrated power stage in GaN. The monolithically integrated half-bridge operates from 500 V and achieves switching frequencies of 6.25 MHz – a record performance. The group demonstrates the record circuit in a totem pole converter with power factor correction.

Galliumnitrid (GaN) is best known for its use in mobile phone chargers, but the requirements for power supplies for devices that consume more power, such as PCs, larger tablets or displays, are quite different. Prof. Dr.-Ing. Bernhard Wicht, from the Institute for Microelectronic Systems at the Leibniz University of Hanover, explains: "In contrast to the usual mobile phone chargers, which are specified for a power between 5 and 20 W, power supplies with 200 W have completely different requirements. It starts with the topology, because a power of around 200 W usually requires a DC link voltage. Specifically, this means that you first convert from the AC voltage to a 400-volt DC-link voltage and then step it down from there. In addition, power factor correction (PFC) is mandatory in such power supplies; the standards require it."

He and his students have set themselves the goal of developing a power supply unit for the 200 W power class based on GaN. This would enable the power supplies used to date to be significantly smaller on the one hand, and to achieve a higher efficiency on the other. Wicht: "And both are possible with GaN." Wicht and his team of developers are thus addressing a market that is not without interest, because "grid-fed electronics consume TWh of energy annually," Wicht continues.

The first step has been taken

At this year's ISSCC in San Francisco, the developers presented a fully integrated GaN-on-SOI-based (silicon-on-insulator) circuit to be used in a power factor correction totem pole topology (TPPFC) that can handle up to 55 W. The fact that less than 55 W has been achieved so far is due to the selected TPPFC system and corresponding design.

GaN as a semiconductor material for ICs is not yet as mature as silicon and this also applies to the 650 V GaN-on-SOI technology from imec used for the development. "We still have to struggle with unpredictable process variations and unfavorable analog properties such as matching etc.," Wicht continues. But: "In the meantime, we have developed concepts and solutions for this and are confident that the next test chip, which we are currently realizing, will achieve 200 W and even more functionality."

Despite the initial difficulties, Wicht is convinced by the GaN-on-SOI technology, because this technology has advantages, for

example, that both high-side and low-side can be implemented on a common substrate. Wicht continues: "GaN-on-SOI is really brilliant, because GaN is free of bipolar effects and with SOI various circuit functions can be integrated on-chip, leading to small parasitic elements, allowing for faster switching. I don't think we would be able to break the record with 500 volts and 6.25 MHz without SOI."

High integration density, high clock frequency

The fully integrated 500 V power stage includes a level shifter, gate drivers and power FETs on a single die. In addition, very high clock frequencies can be used. The established players in the GaN market typically work in the 1 MHz range. "We actually went up to 6.25 MHz with our integrated half-bridge at 500 volts. Both values have been validated and that is still a world record," says Wicht. In addition, the development is characterized by excellent waveforms, according to Wicht. "The high integration has greatly reduced the parasitic effects, and the inductive effects are also low, which in turn reduces ringing. This simply shows the potential of GaN."

The GaN IC is used in a TPPFC system based on the TPPFC 1680 controller from Onsemi, so the overall system could not be clocked as high.

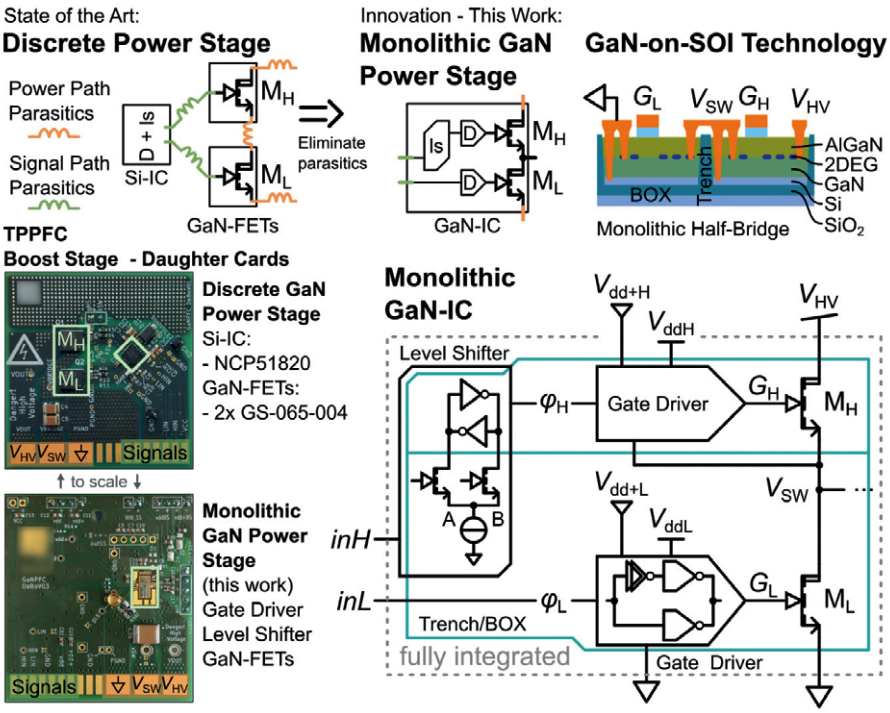


Figure 31.10.2: Discrete versus monolithic GaN power-stage and block diagram of the implemented GaN-IC.

Further development is assured

Further development is being driven forward by the DFG (German Research Foundation) as part of the priority program "GaNius". One of the issues here is to find out which clock frequency really makes sense from a technical point of view, "because it is now clear that we can clock very high", Wicht continues. In addition, the focus is of course on integrating further functions, such as a closed control loop on the die. "Driving system integration using advanced packaging technologies is also an approach we are looking at. For example, we would also like to integrate the passive

Bernhard Wicht, Leibniz University Hanover: "With our half-bridge integrated in GaN and 500 V, we were able to achieve a frequency of up to 6.25 MHz. That is an absolute world record, no one has ever managed that before."

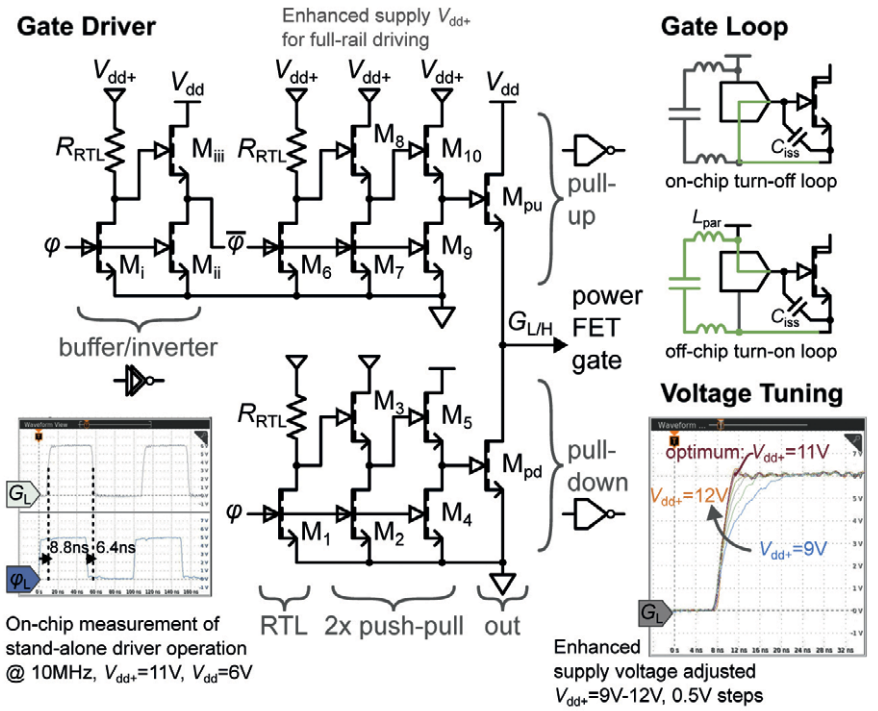


Figure 31.10.3: Schematic and measured waveforms of the implemented monolithic GaN gate driver.

Image: ISSCC Digest/Leibniz University Hanover

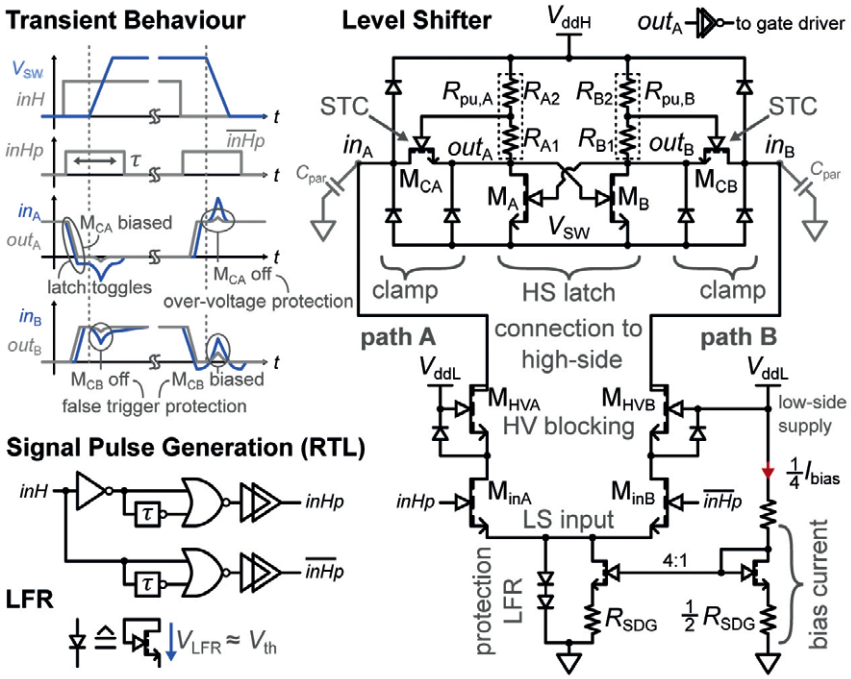


Figure 31.10.4: Schematic and operation principle of the high-voltage level shifter with series transitor clamp (STC) high-side protection circuit and pulsed input signal.

components," explains Wicht. However, the first step is to get the most out of the monolithic approach.

Details from the ISSCC paper

The paper 31.10 with the title "A Fully integrated 500 V, 6.25 MHz GaN-IC for Totem-Pole PFC Off-Line Power Conversion« presents a TPPFC converter that benefits from a monolithic GaN-IC with a fully integrated half-bridge power stage in a 650 V GaN-on-SOI technology.

A 650 V GaN-on-SOI technology utilizes trench isolation and buried oxides (BOX), allowing the integration of the entire power stage on one single die. Figure 31.10.2 (top right) depicts the cross-section. Besides the HV transistor, the technology offers a low voltage transistor, a 2DEG resistor, and a capacitor. A d-mode device is not available, and generally, no p-type device. The PCB photos in Fig. 31.10.2 show the monolithic ML/MH half-bridge daughter board and, for comparison, the discrete design used in the TPPFC system. The monolithic implementation reduces component count and footprint size. Figure 31.10.2 (bottom right) shows the GaN-IC of this work comprising split-path gate drivers and a half-bridge with equally sized 500 mΩ power FETs to ensure symmetric operation in positive and negative half-line cycles of the TPPFC operation. A cross coupled level shifter with robust HV capability interfaces the high- and low-side domains. The high-side rails V_{ddH}, V_{dd+H} are generated by bootstrapping from the low-side supplies V_{ddL}, V_{dd+L}.

With the lack of p-type devices, topology choice is crucial in GaN gate driver design. The implemented full-rail gate driver in Fig. 31.10.3 relies on a split-path approach with separately controlled paths for M_{pu}, M_{pd}. Each path consists of an RTL inverter followed by two subsequent push-pull stages showing tapered drive strength and minimized static power consumption (R_{RTL} = 59 kΩ). The push-pull stages employ n-type devices in the pull-up path, inherently limiting the output high-state to $V_{out,high} \leq V_{in,high} - V_{th}$. An enhanced supply voltage V_{dd+} is applied to the respective stages, ensuring full turn-on of M_{pu} when the gate driver output $G_{H/L}$ is pulled high, resulting in full-rail driving. The gate driver achieves rise/fall times of 3.5/2.7 ns with less than 2 % overshoot, switching at 10 MHz, as shown in Fig. 31.10.3 (bottom left). The propagation delay is 8.8/6.4 ns for the rising/falling edge, faster than other comparable approaches. Monolithic integration significantly improves the power-FET gate loop. However, some inductance remains in the turn-on path; see Fig. 31.10.3 (top right). The gate driver facilitates a voltage tuning technique, allowing to adjust V_{dd+} to limit the parasitic loop induced gate voltage overshoot at the power-FET gate. Based on the on-chip measurements in Fig. 31.10.3 (bottom right), V_{dd+} = 11 V is selected as a trade-off between rising edge slope and overshoot.

Image: ISSCC Digest/Leibniz University Hanover

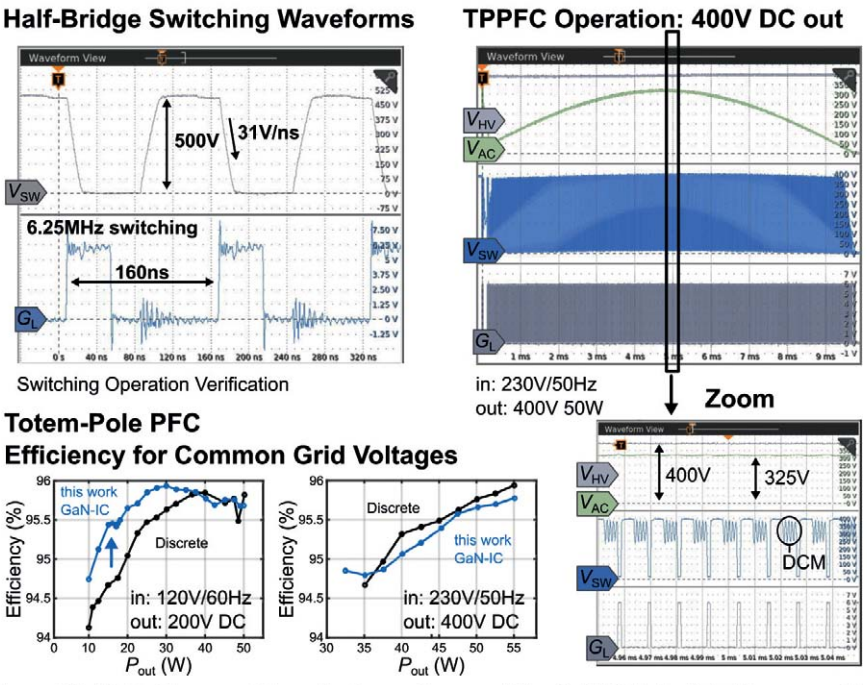


Figure 31.10.5: Measured transient waveforms of the GaN-IC in half-bridge operation and in the TPPFC; measured TPPFC-efficiency with GaN-IC vs. discrete implementation at 120 V/60 Hz and 230 V/ 50 Hz.

Figure 31.10.4 shows the level shifter implemented on the GaN-IC. At the high side, a cross-coupled RTL-inverter latch holds the logic

	ISSCC 2020 [2]	ISPSD 2020 [3]	APEC 2021 [4]	ISSCC 2022 [5]	ISSCC 2022 [6]	This Work	
						Discrete	GaN-IC
Technology	650 V e-mode GaN-on-Si	650 V GaN-on-Si	200 V GaN-on-SOI	e-mode GaN-on-SOI	500 nm GaN-on-Si	Discrete GaN on PCB level	650 V GaN-on-SOI
Voltage V_{HV} (V)	60-400	200	180/130*	48	48/400	400	500
Power Stage (HEMT + Driver)	integrated	integrated	integrated	integrated	integrated	discrete	integrated
Level Shifter	integrated, low-side only	external	integrated* (separate die)	integrated	n.r.	external	integrated
Switching frequency (MHz)	0.262	1.5 (open-loop boost)	5/1*	0.5	50/12.5	<0.275 (closed-loop)	6.25 (open-loop)
Rise/fall time driver (ns)	n.r.	n.r.	sim: 6.0/3.2 meas.:2.0/n.r.	n.r.	n.r.	13.4/1.1	3.5/2.7
Gate driver rise/fall propagation delay (ns)	50/n.r.	n.r.	sim: 8.1/10.6	11.6/14	n.r.	8.2/60	8.8/6.4
Switching node transition slope (V/ns)	n.r.	25	peak: 112 (low-side only)	n.r.	average: 120	average: 2-3	average: 31 peak: 75
Active die size (mm²)	2.1	n.r.	n.r.	4.5	16.75	not applicable	6.6
Application	Off-line buck converter	Totem-Pole PFC	Demonstrator	48V-to-1V conversion	48V-to-5V conversion	Totem-Pole PFC	Totem-Pole PFC

n.r. = not reported, * stand-alone level shifter on separate die, characterized at 130V, 1MHz

Image: ISSCC Digest/Leibniz University Hanover

Figure 31.10.6: Comparison of the implemented GaN-IC and its sub blocks with the discrete PCB power stage and state-of-the-art designs.

state. Directing a bias current I_{bias} (600 µA) through either M_{inA} or M_{inB} pulls inA or inB low, activating M_{CA}/M_{CB}. This pulls down the corresponding $out_{A/B}$ node, toggling the latch. out_A is connected to the HS gate driver input via an inverter acting as a buffer. To minimize losses due to I_{bias}, the input signals are applied in a pulsed manner, accomplished by RTL logic and an R-C delay. I_{bias} is generated by a current mirror employing a source degeneration R_{SDG} to account for threshold voltage variation. HV cascodes M_{HVA} and M_{HVB}, referred to V_{ddL}, and lateral field-effect rectifiers (LFR) protect the low-side circuits from the high voltage at $in_{A/B}$. Due to the parasitic capacitance, C_{par} at in_A and in_B (marked in Fig. 31.10.4), the HV transient at the switching node V_{sw} can cause critical over-voltage stress at the gates of M_A and M_B. As a key innovation of the proposed level shifter, a series transistor clamp (STC) formed by M_{CA} and M_{CB} protects M_B and M_A. V_{dd} is typically chosen close to the $V_{GS,max}$ rating of the GaN-FETs; hence, clamping to $V_{dd}+V_{LFR}$ is insufficient. The proposed STC achieves protection by reusing the pull-up resistors of the latch to control the gate of M_{CA} and M_{CB}, illustrated by the transient curves in Fig. 31.10.3 (left). For out_A at high state (= V_{ddH}), M_{CA} disconnects out_A from in_A with its source and gate nodes pulled to V_{ddH} via R_{A1}, R_{A2} while M_{CB} is activated to prevent false triggering by disturbance at in_B. In low-state (out_A at V_{sw}), the STC limits $V_{(outA)}$ to $(V_{ddH} - V_{sw}) \cdot R_{A1}/(R_{A1}+R_{A2})-V_{th}$, protecting the gate node of M_B from over-voltages. The resistive divider ensures that the STC kicks in earlier, maintaining the max. ratings of M_A and M_B. Accounting for C_{par} of up to 100 fF, R_{A1}/R_{A2} and the widths ratio $W(M_{CA})/W(M_A)$ are chosen 2:1, similarly, for path B.

Figure 31.10.5 shows the transient measurement results of the switching GaN-IC. The half-bridge and, thus, the level shifter is verified to operate at 500 V and frequencies up to 6.25 MHz (upper left), achieving an average V_{sw} slope of 31 V/ns. The GaN-IC is applied in a TPPFC system based on the onsemi 1680 TPPFC controller, converting the AC input to V_{HV} = 400 V (DC) (Fig. 31.10.5 right). The zoomed section shows the instantaneous AC voltage close to the peak of 325 V and the low-side gate voltage. Also, the DCM-related ringing of V_{SW} is visible. The TPPFC is operated in two standard grid configurations and compared to the discrete power stage of Fig. 31.10.2 (center left): 120 V – 60 Hz (V_{HV} = 200 V) and 230 V – 50 Hz (V_{HV} = 400 V). The efficiency curves in Fig. 31.10.5 (bottom) confirm the higher efficiency of the GaN-IC at lighter loads as it is switching-loss optimized.

The GaN-IC is fabricated in a 650 V GaN-on-SOI technology using an active area of 6.6 mm² (Fig. 31.10.7). The IC utilizes the advantages of monolithic GaN integration, providing miniaturization, lower internal and external parasitics and high design flexibility. mk

Europe and semiconductors

"The costs for having a test chip manufactured are around 30,000 euros for us, and even more than 100 k euros, for advanced nodes," explains Prof. Dr.-Ing. Bernhard Wicht, who works at the Institute for Microelectronic Systems at the Leibniz University of Hanover. And that is precisely where a major problem lies, because universities cannot afford this often. That is why Wicht is convinced that this point must also be addressed by the EU or Germany, i. e. financial support from the government. "When I talk to colleagues from universities in China or Taiwan, they either don't have to pay anything or a minimal price, the rest is subsidized by the state. While we are still discussing the costs here, whether we can make a chip, they have already made 10 chips."
This is also important because the European Chips Act is also about the universities training the corresponding semiconductor developers. Wicht explains that his university, thanks to its reputation, "attracts great people but currently held back from reaching its full potential. Because the costs of chip production are a big problem for European/German universities."

A Digital Twin approach for online impedance-based stability analysis

Sergio de Lopez Diz, Roberto Martin Lopez, Francisco Javier Rodriguez Sanchez, Member IEEE, and Emilio Jose Bueno Peña, Senior Member IEEE.

This year, a research paper from the Department of Electronics, Escuela Politécnica Superior, Universidad de Alcalá, Madrid, Spain, was published by IEEE Xplore that highlights the advantages of digital twins in power distribution systems.

This IEEE Xplore paper from researchers at the Universidad de Alcalá, Spain, presents a comprehensive study on the application of Digital Twins (DT) for real-time, online impedance-based stability analysis in power distribution systems. The research explores how digital twins can be used to address stability challenges in power distribution, where advanced networks with multiple parallel inverters create complex dynamics that require precise monitoring and control.

Challenges for the stability of power distribution systems

In modern power systems, particularly those integrating renewable energy sources, many inverters often operate in parallel within a network, generating stability concerns due to dynamic interactions. This paper's main focus is on improving the real-time stability of three-phase AC systems through small-signal analysis, which involves examining the impedance interactions between power sources and loads. Typically, the stability of these systems is assessed by calculating the source-to-load impedance ratio in the dq plane, using the Generalized Nyquist Criterion (GNC) as a stability metric.

The DT concept (Figure 1), as applied here, allows the creation of virtual models that represent physical systems with high accuracy and real-time response, capturing data from ongoing operations to predict behavior and potential instabilities. The study's DT-based methodology enables not only stability monitoring but also dynamic control and fault mitigation by continuously updating with real-time data through edge-computing platforms. The paper describes how broadband excitation methods based on pseudorandom binary sequences (PRBS) and Fourier techniques are applied to generate impedance measurements and real-time stability metrics.

Advantages of Digital Twins in power system stability

The integration of DTs enables a real-time view of stability metrics, which is crucial in power systems with parallel inverters due to their continuous dynamic interactions. Traditional stability analysis methods, often based on parametric or nonparametric models, come with significant limitations: parametric models require pre-set parameters that can miss real-time fluctuations, while nonparametric approaches require complex disturbance injections that are impractical for real-time applications. DTs, however, enable adaptive, real-time responses, as they

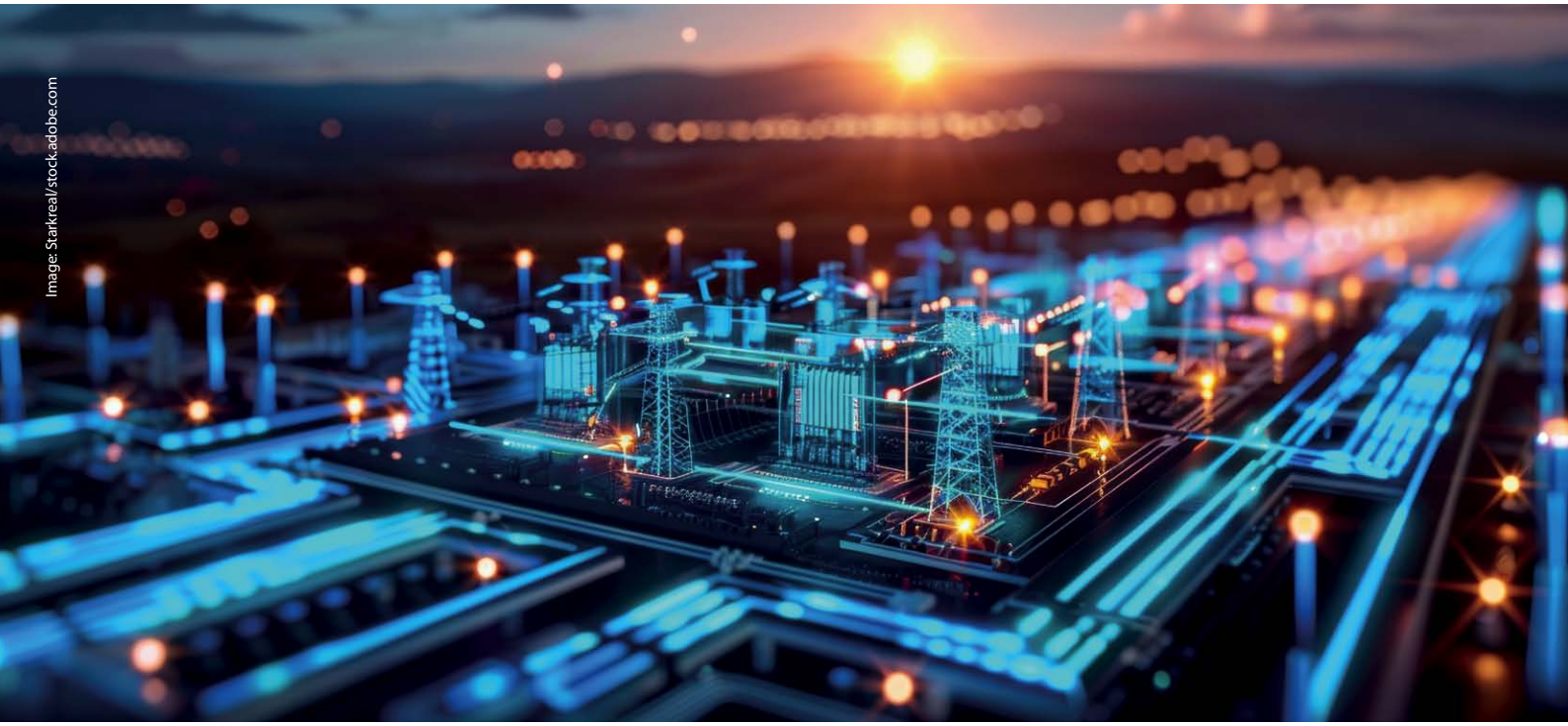


Image: Starkreal/stock.adobe.com

incorporate all physical and control components within a digital replica of the system (Figure 2).

DTs provide a flexible solution for stability analysis by continuously adapting to changing conditions without the need for offline linearization. In scenarios where environmental and system factors are constantly fluctuating, such as in renewable energy sources, DTs offer a method to track real-time stability without disrupting the physical system.

Real-time stability monitoring on edge computing platforms

The DT architecture implemented in this study runs on an edge-computing platform, allowing real-time monitoring of two three-level converters: one grid-forming (GFM) and the other grid-following (GFL) (Figure 3). This architecture is based on a Zynq edge-computing board with dual Arm cores and programmable logic, supporting both the physical system and the digital replica on a single control board. With the GFM converter regulating output voltage and the GFL converter adjusting current to match the grid, the setup effectively illustrates how DTs can monitor and manage complex stability challenges.

In this setup, sensor inputs from the physical system – such as DC bus voltage and LC filter output currents – feed directly into the DT. Simultaneously, two perturbation sequences are introduced into the DT's dq channels: Maximum Length Binary Sequence (MLBS) and Inverse Repeat Sequence (IRS). These PRBS signals enhance efficiency by using orthogonal designs that minimize interference and expedite the measurement process. By implementing the DT on an edge-computing platform, the system maintains closely synchronized with real-world operations, enabling accurate and responsive adjustments to control parameters in real time.

Digital Twin as a tool for enhanced system stability

This paper demonstrates that a DT can be used to derive real-time stability metrics, such as phase margin, across all feasible operating points of the physical system without needing linearization. The DT's real-time capabilities support adaptive, online identification of stability parameters, meaning that the DT can respond dynamically to changes in operating conditions. This ability to capture nonlinear effects in real time, such as dead time, conduction, and switching losses, makes the DT approach well-suited for real-world applications.

Key to this capability is the DT's integration on the same control board as the physical system, allowing simultaneous and consistent control of both domains. This setup facilitates observing how system nonlinearities affect stability, with DT continuously updating the stability analysis based on ongoing measurements from the physical system. Additionally, the DT allows for pre-implementation testing of control adjustments, helping to ensure that changes in the control structure do not negatively impact system stability.

Impedance-based stability analysis with DTs

To estimate the source-to-load impedance, which is crucial for real-time stability monitoring, the DT applies a set of orthogonal perturbations in the dq reference frame. Two types of binary perturbation sequences are used to determine the impedance ratio in both the digital and physical domains, allowing stability analysis based on real-time Nyquist plot monitoring. These sequences (MLBS for the D channel and IRS for the Q channel) are injected into the DT model and physical system simultaneously, allowing stability margin calculation in a single step.

This impedance-based approach enables a comprehensive analysis of the system's stability by examining the Nyquist plot, which reveals how system stability responds to changes in control parameters. Additionally, this technique enables the detection of specific instability points by applying the GNC to eigenvalues in the characteristic equation of the system. For example, by reducing the GFM converter's control bandwidth, the researchers could induce oscillations and observe real-time stability degradation, demonstrating the DT's efficacy in stability prediction.

Technical challenges and optimization

The DT implementation on an edge-computing platform requires several technical optimizations. Given the system's high-frequency processing requirements, the DT's time step is set at 2.5 microseconds to ensure that it remains responsive to rapid changes in the physical system. This short time step ensures that the DT can operate synchronously with the physical converter, making it possible to perform stability analyses without delays. However, the platform's non-preemptive nature and multiple interrupt sources required careful management. In this setup, control interrupts were set at 100 microseconds, with the DT interrupt operating at a higher frequency to minimize the risk of step loss.

Another key optimization is in the design of the PRBS perturbations. These sequences provide high power while respecting amplitude constraints, allowing for an optimal balance between signal-to-noise ratio and real-time accuracy. By applying orthogonal binary sequences, the DT's measurement time is minimized without losing impedance

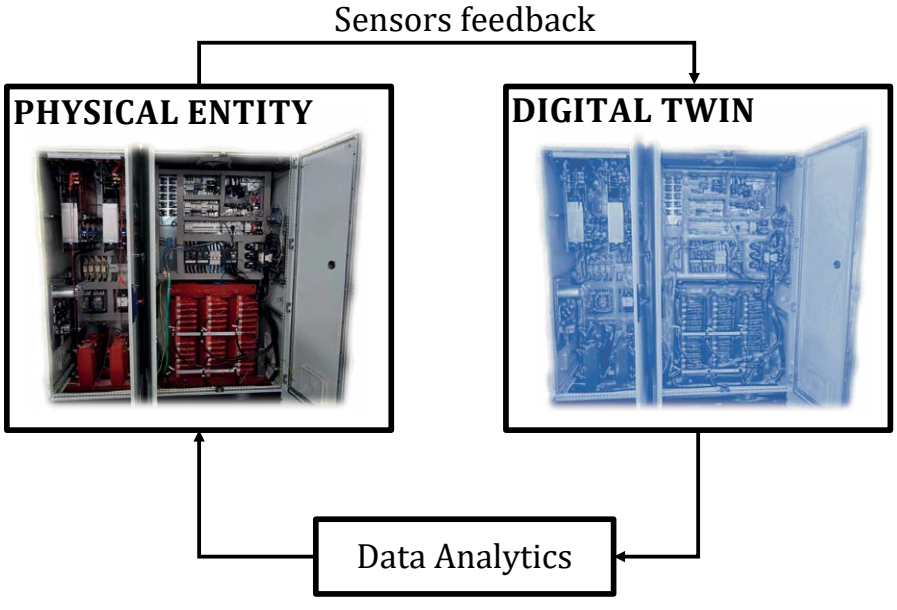


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Figure 1: Example of DT technology applied to a power electronics converter

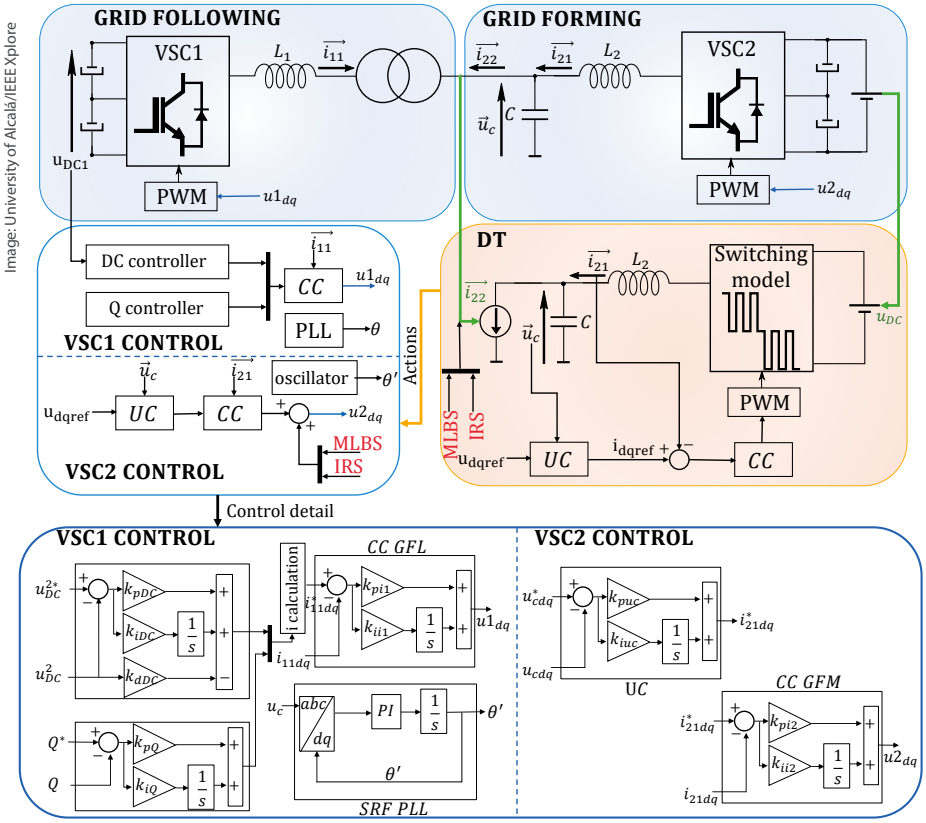

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Figure 2: Experimental system setup for the real-time stability analysis based on DT

estimation accuracy. The MLBS sequence has a frequency resolution of approximately 1.2 Hz, and the IRS sequence, being twice as long, provides a detailed frequency response profile across the dq channels.

Real-time experimental validation

The experimental setup for validating this DT approach included two hybrid dual-mode converters: a GFM system with adjustable bandwidth control and a GFL system with fixed parameters. Three test cases were evaluated to demonstrate stability metrics and the impact of bandwidth adjustments on system stability. The experiments showed that reducing the GFM's bandwidth created conditions for instability, allowing researchers to track stability loss in real time through Nyquist plots and eigenvalue frequency response data.

The DT's measurements indicated that the phase margin decreased as bandwidth narrowed, with critical instability points detected accurately by the DT analysis. Time-domain analysis showed that as bandwidth dropped, transient response oscillations persisted longer, closely matching the Nyquist-based stability predictions.

Additionally, the DT's ability to support adaptive control is illustrated by its response to oscillations resulting from PLL-induced instabilities, which arise when the GFM operates within a weak grid. By tracking eigenvalue responses, the DT accurately detected and reported low-frequency phase shifts that indicate impending instability.

Using these real-time metrics, the DT could suggest controller adjustments, such as bandwidth expansions, which were validated within the DT model before implementation in the physical system.

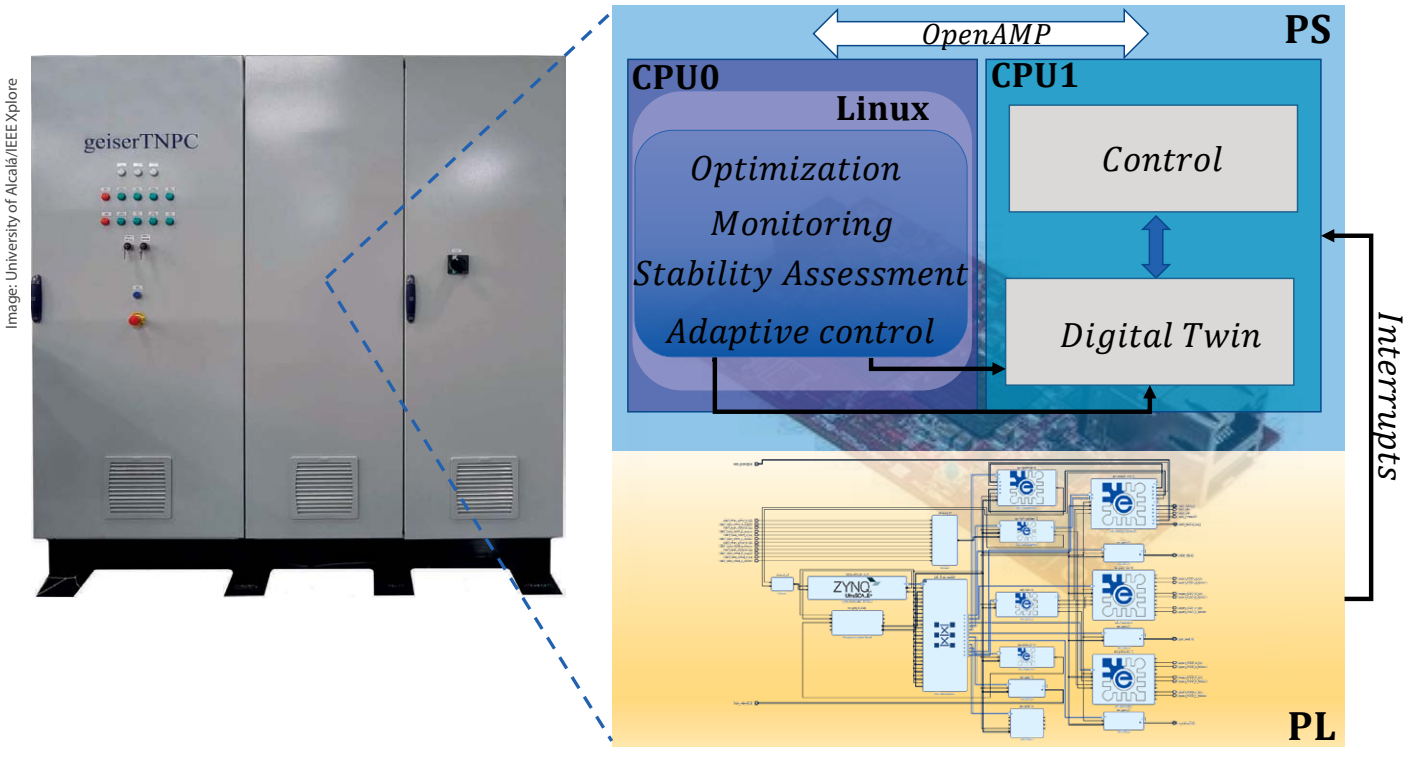

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Figure 3: Implementation of the DT on an edge-computing platform

Implications for adaptive control in power distribution

A central benefit of the DT approach is its capacity to support adaptive control by providing real-time stability insights that enable dynamic parameter adjustments. Unlike static gain scheduling, which relies on predefined system conditions, this DT-based approach allows continuous stability monitoring and adaptive control in response to load and system impedance variations. This ability to adapt control strategies dynamically makes the DT approach particularly useful in scenarios with unpredictable grid conditions, such as wind farms or remote installations where grid parameters may vary.

Beyond stability monitoring, the DT enables continuous condition monitoring and fault detection, enhancing system reliability and safety. By consistently evaluating real-time stability margins, the DT can identify patterns that signal emerging faults, providing an opportunity for proactive maintenance. This approach aligns with the growing demand for intelligent monitoring systems in distributed power networks, where stable and efficient power delivery is critical.

Previous research

Already 2022 a paper was published by Elsevier which explores using Digital Twin (DT) technology for monitoring and maintaining the stability of three-phase power converters, essential in the energy transition toward renewable sources. Key components like Voltage Source Converters (VSCs), operating with LC filters to suppress harmonics, are vital for grid integration. The DT approach provides a real-time virtual replica of the physical converter, utilizing edge computing to enable condition monitoring of LC filters and predicting component wear (Figure 4).

By incorporating Particle Swarm Optimization (PSO) and Genetic Algorithms (GA), the DT model precisely estimates degradation, supporting adaptive control strategies and predictive maintenance. This setup allows close matching of DT output with real-world signals, enabling proactive adjustments before failures. The study demonstrates the feasibility of deploying DTs in low-cost, edge-computing environments, offering a new avenue for reliable, cost-efficient monitoring and extending the lifespan of power converters. The DT's successful real-time monitoring on a low-cost platform marks significant potential for broader application across more complex converter systems.

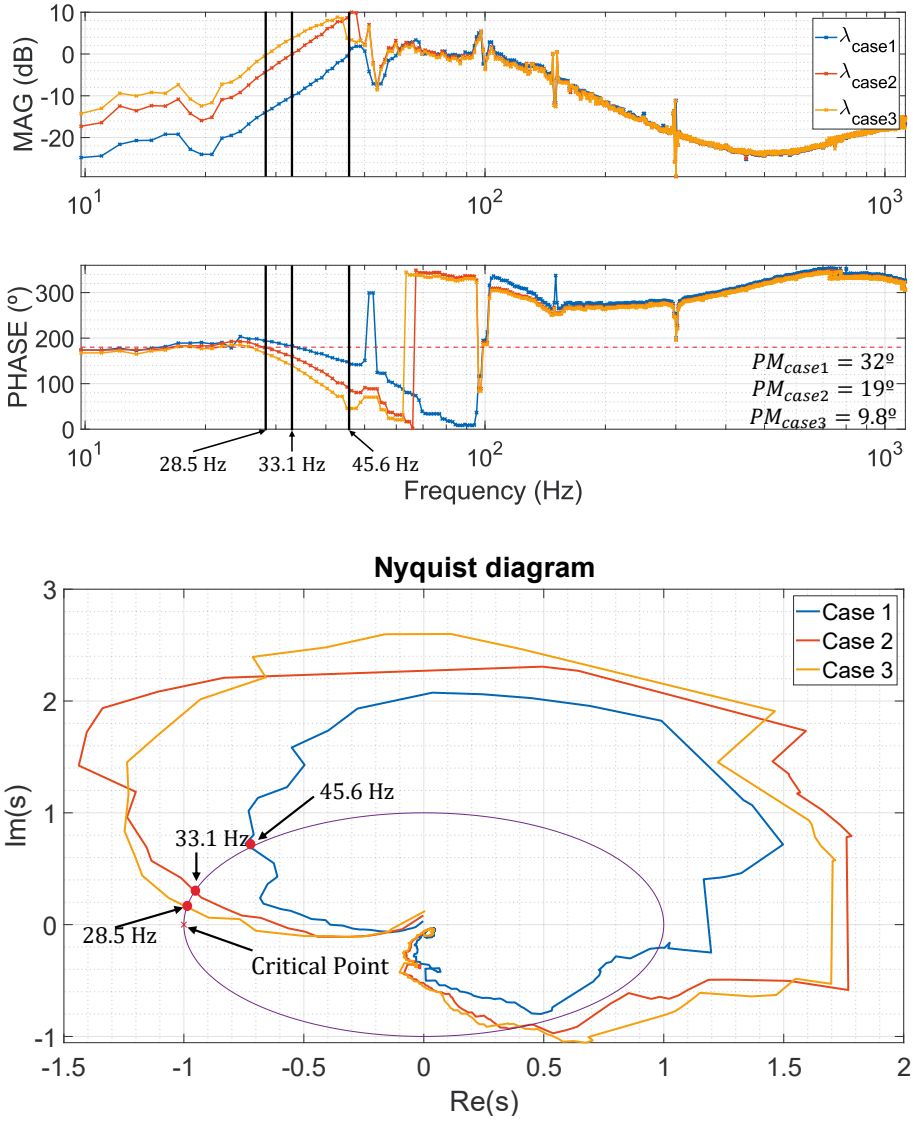

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Figure 4: Experimental results of the real-time stability assessment: (a) Eigenvalues of the minor loop of source/load impedance, (b) equivalent Nyquist diagram

Conclusion

This last study showcases the DT approach as a practical tool for real-time stability analysis and adaptive control in distributed power systems. The experimental results highlight how DTs can offer similar output waveforms to their physical counterparts, demonstrating accuracy in real-time stability analysis. The DT's ability to work on cost-effective edge-computing platforms underscores its potential for widespread adoption in renewable energy and other distributed power environments.

Future research could expand DT applications to include dynamic stability assessments, such as voltage dips or overvoltages, by training DTs to respond to diverse perturbations. The model could simulate various grid conditions and disturbances, providing comprehensive insights into the converter's dynamic responses and stability. Additionally, DT technology could further develop to incorporate advanced fault prediction capabilities, creating a fully autonomous stability monitoring and control system.

In summary, this research establishes DTs as a powerful solution for addressing stability challenges in advanced power distribution networks. By providing real-time, high-fidelity monitoring and control, DTs mark a transformative shift in how stability is managed in energy systems, paving the way for the next generation of digitalized, adaptive power networks. st

Medium voltage – a resource-efficient way to interconnect

Dipl.-Ing. Christian Schöner, Business Development Manager Power Electronics and Grid Integration Power Solutions, Fraunhofer Institute for Solar Energy Systems ISE

To meet CO_2 reduction targets, renewable energy use, especially PV must increase significantly. Medium voltage (MV) could help to reduce raw material needs (copper, aluminum) and costs, could support larger power outputs, and optimizes hybrid systems – a real chance for European companies.

Image: Wuttichai/stock.adobe.com

CO_2 emissions must be significantly reduced by 2050. To achieve this, we need a big increase in renewables. For photovoltaic, an increase of around 73 TW in installed capacity alone is expected worldwide. Additionally, the electricity, heating and mobility sectors will be electrified, with the electricity grid becoming the hub for sector coupling. Using today's technology, large amounts of raw materials like copper and aluminum will be required to connect the different areas of energy provision, storage, distribution and utilization. According to the International Energy Agency's "Global Critical Minerals Outlook 2024", copper demand will exceed the available supply from 2025 on, and thus raw material prices are expected to rise in the future. The European Union also identified in the "Study on critical raw materials for the EU 2023" aluminum as further critical raw material with a high economic importance and a high supply risk.

Increasing the system voltage can be one solution, as it simultaneously reduces the current, potentially resulting in substantial savings in material, costs and space. However, medium voltage (MV) technology is the key to open the resource-efficient integration of renewables in the energy system. This technology also allows new system concepts for renewable hybrid power plants whose individual components are interconnected via medium voltage.

Motivation for developments towards higher voltage levels

The PV industry is subject to enormous cost pressure. This is one of the reasons why considerable investment has been made in the further development of this technology in recent years. The price per installed kWp has dropped by about 14% per year over time, due to advances in technology and economies of scale in production. Today the costs for the installation and BoS hardware account for over 40% of the total costs. In future, savings in these areas will have a greater impact on the overall price. Medium voltage is a key lever in reducing energy generation costs.

Higher system voltages result in reduced cable currents, leading to savings in many areas. For example, the cable cross-sections can be greatly reduced, thus saving raw materials like copper and aluminum. As shown in Figure 1 doubling the output voltage leads to halving the output current and to a 75% reduction in cable cross-section, considering only the pure current carrying capacity of a single conductor. However, the material costs are not the only savings potential for cables. Installation costs can be saved by smaller cables as well, since they are generally easier to lay and connect.

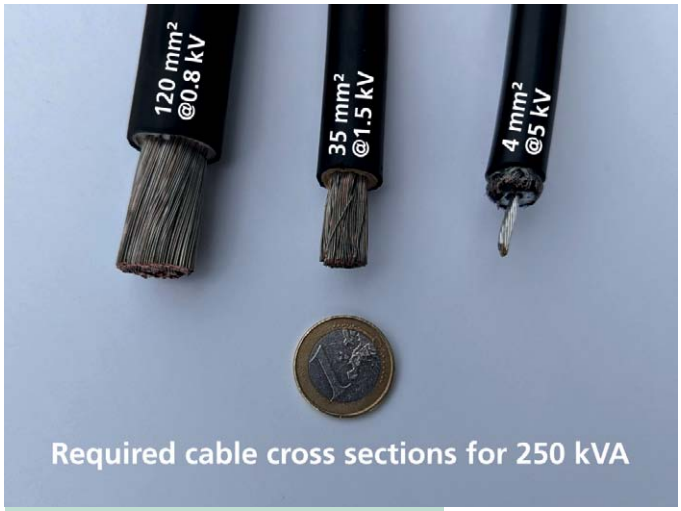

Figure 1: Minimum cable cross-sections for 250 kW PV inverter at different voltage levels.

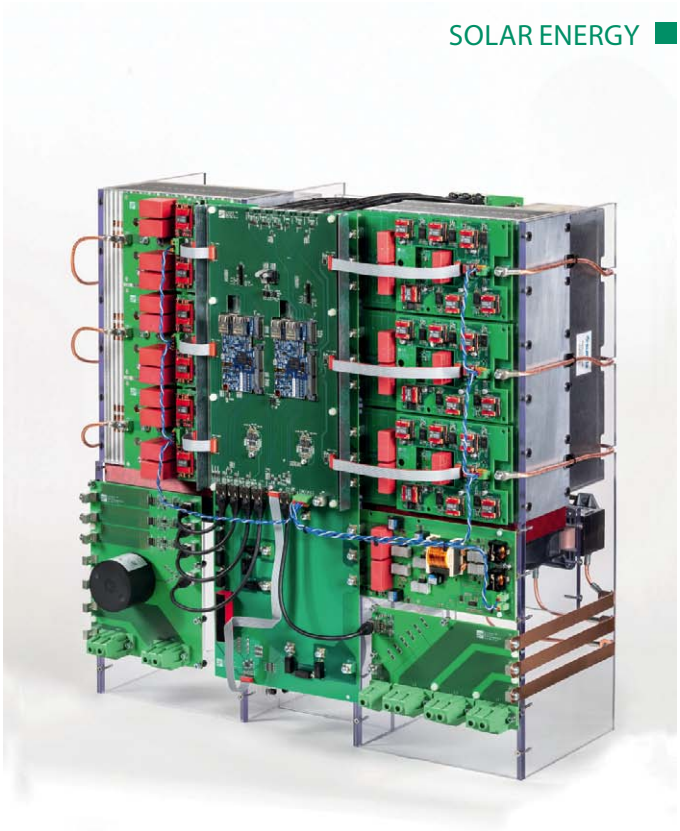

Figure 2: Medium voltage string inverter for future utility-scale PV power plants. Output power 250 kW, Output voltage 1,500 V (AC), PV voltage 1.7 kV (DC) to 2.4 kV (DC).

Another advantage of medium voltage is that higher voltages allow to increase the power of the individual subsystems. Today's PV power plants mostly use subsystems between 3 and 5 MVA in size, whose output cannot be significantly increased due to the large copper cross-sections necessary for the current in the low voltage range. By switching to medium voltage, a transformer with the same cross-section can transmit a higher power (10 – 12 MVA at 1,500 V). For PV power plants of the same size, the plant with medium voltage technology requires a smaller number of transformers and switchgears. This leads to lower construction measures and installation costs, while freeing up space for additional PV modules at the same time.

State of the art in research and technology

In the early days of silicon carbide (SiC) semiconductor development, there was great euphoria for the technology, and the advantages of wide bandgap devices were demonstrated in a wide variety of components. These included components with blocking voltages up to 25 kV. Even back, higher voltages were being considered in the field of PV and first research projects.

However, the costs of the new semiconductors were still too high, and the technology was still plagued by various teething troubles resulting that components with high blocking voltages were still too far away from being ready for serial production. With the rise of e-mobility and the increasing demand for SiC components < 1.7 kV, all manufacturers focused on optimizing these voltage classes. The further development of higher voltage components came to a standstill.

SiC has now fully arrived in e-mobility. More manufacturers are once again focusing on higher voltage classes. 3.3 kV devices are available on the market from various manufacturers and 6.5 kV is well on its way to serial production. In the meantime, various research projects have shown that the construction of highly efficient inverters based on medium voltage SiC devices is technically feasible.

Researchers at Fraunhofer ISE have developed the world's first medium-voltage PV string inverter and successfully put it into operation on the grid, as shown in Figure 2. It was developed as part of the public funded "MS-LeiKra" project. The PV inverter has an output voltage of 1,500 V (AC) with an output power of 250 kVA realized in a two-stage design. The step-up converter with a PV input voltage of 1.7 kV (DC) to 2.4 kV (DC) is based on 3.3 kV SiC devices. The inverter section was constructed using hybrid ANPC (Active Neutral Point Clamped) power modules. Four silicon and two SiC semiconductors are used. This topology allows to use the major advantages of SiC.

Higher voltages are also possible. A three-phase converter with 3 kV (AC)/250 kVA was also developed at Fraunhofer ISE as shown in Figure 3 in the public funded project "SiC-MS-Bat". The converter unit can be connected in parallel on the DC and grid side, each with its own LCL filter. It is an ANPC topology used with 3.3 kV SiC devices, using three half-bridge modules per phase. The switching frequency of the transistors is 16 kHz. The PWM-pattern of the ANPC generates a ripple frequency of 32 kHz for the alternating part of the current. This helps to decrease the filter effort. Depending on the design of the inverter, up to 2 MVA can be realized in a control cabinet with a floor space of 80 x 80 cm^2.

Current situation and the market

The mentioned projects show that the technological course has been set for the transition to medium voltage. At the same time, the technical innovation potential for PV in the low-voltage range is heavily saturated. Technological advances and thus unique selling points are only possible to a very limited extent, making price the main selling point. This poses major challenges for European manufacturers.

The market situation and the rising raw material prices in recent years have increased the pressure to innovate. In the meantime, there have been initial advances in the direction of higher voltages. One example is the "Mengjiawan"

project in the Shanxi province of China. Here, a pilot power plant with a DC voltage of 2,000 V was built and put into operation.

The researchers at Fraunhofer ISE are now convinced that it is no longer a question of whether the medium voltage technology will be introduced, but rather who will be the first players in this promising market and thus determine the technology. As already shown, the global demand for installed PV power will be 73 TW by 2050. The share of utility-scale power plants, and thus the area of application for medium voltage, will be between 40 and 60%. This is a great opportunity for European manufacturers to regain technological leadership, at least in utility-scale power plants.

The issue of standardization and overcoming obstacles together

Despite the steadily increasing output power of PV inverters, the increase in system voltage has stagnated since 2018. This is due to the definition of low voltage, which ends at 1,500 V (DC) or 1,000 V (AC). All existing PV standards up to now refer to this limiting value. An increase beyond this value is currently hindered by the existing standards, as they must first be adjusted, or rather extended, to meet the basic standards for medium voltage applications. The good news is, that standardization committees are already looking into the higher voltages and first drafts for PV up to 3 kV are already written.

A European consortium, made up of representatives from all trades involved in large utility-scale PV power plants, has been formed to jointly address and compile the technological and normative requirements necessary for the leap to medium voltage. This powerful consortium that is open to additional participants can tackle the existing hurdles together and achieve optimization throughout the entire power plant.

Applicability to other areas

Utility-scale PV power plants are just the beginning. When individual components are linked together in a resource-efficient way via medium voltage, this allows system approaches for hybrid power plants and the integration of decentralized energy generation to be rethought. It enables more resilient district power supplies, charging infrastructures of electrical vehicles or even operation of industrial grids in heavy industry with reduced dependence on the traditional power grid.

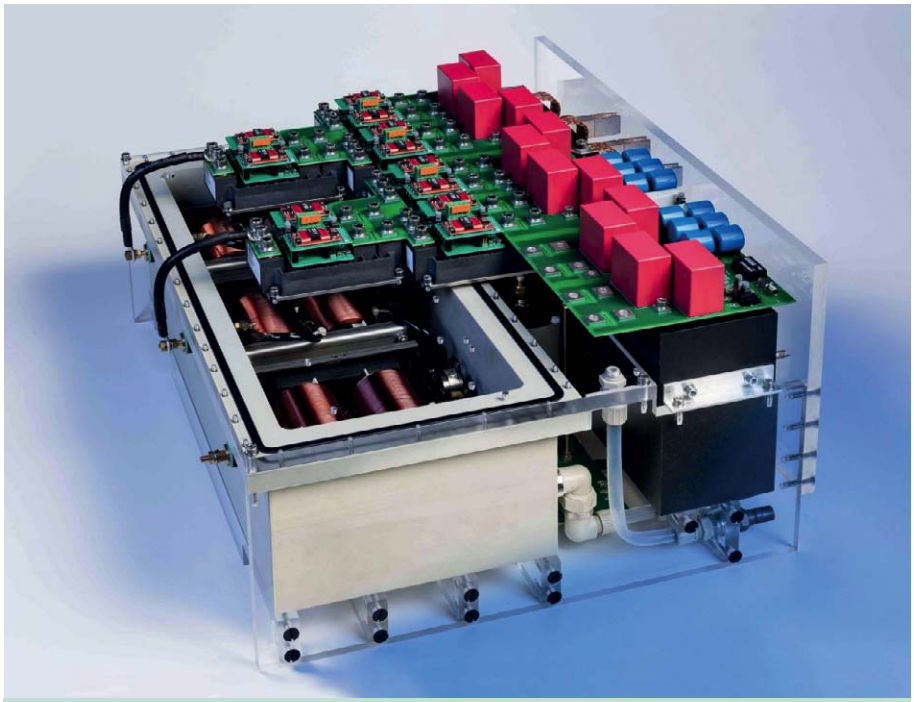

Image: Fraunhofer ISE

Figure 3: A 250 kVA inverter stack with 3.3 kV SiC transistors.

The transition to electric vehicles will be accelerated by the CO_2 reduction target and the EU registration change from 2035, according to which only new cars with combustion engines that no longer emit CO_2 while driving can be registered. While intensive research is being carried out on vehicles and charging systems, little attention is paid to the connection between the charging station and the public grid to the required provision of power. Currently, cars can be fast charged with up to 850 V (DC)/350 kW. In future, trucks will be able to be charged with up to 1,250 V (DC)/3 kA (DC) in accordance with the MCS standard.

The study "Easy Charging at Service Areas" by the German National Center for Charging Infrastructure deals with the power requirements of electric charging stations. The study found that fast-charging systems with capacities ranging from 8 MVA to 26 MVA will be required in the future. The requirement for a charging facility for trucks and cars at least every 50 km along Germany's freeways, which covers total of 13,200 kilometers, translates to a total installed charging capacity in the high double-digit GW range. This estimate does not include large electric charging stations in urban areas and charging stations at trucking companies. For large truck stops with up to 150 parking spaces, the charging capacities at night can add up to 5 – 7 MVA, depending on the assumed simultaneity factor.

To relieve the load on the grids, a combination of storage and renewable generation directly on site is a promising solution. Parking lot roofs offer a large PV potential here. However, the connected load must also be distributed on site and routed to the individual charging points. To achieve a high level of efficiency and limit the use of materials, the move to medium voltage offers a sensible approach. As PV, storage and charging technology are DC-based, an MV (DC) bus system would probably be the most efficient solution in the future.

Summary

Contrary to all the hurdles in the past, the signs are currently looking good for the introduction of medium voltage in PV. The technical feasibility has been demonstrated several times. The first steps have already been taken by various manufacturers and the first pilot systems are already in operation. The problem has also been recognized on the standardization side, and the committees are working on the important normative basis for this step towards resource-saving renewable energy generation. There are a lot of applications where higher system voltages enable considerable material, cost and space savings and open new system concepts for hybrid power plants. Let's push forward towards a high-efficient renewables-based energy transition together! st

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