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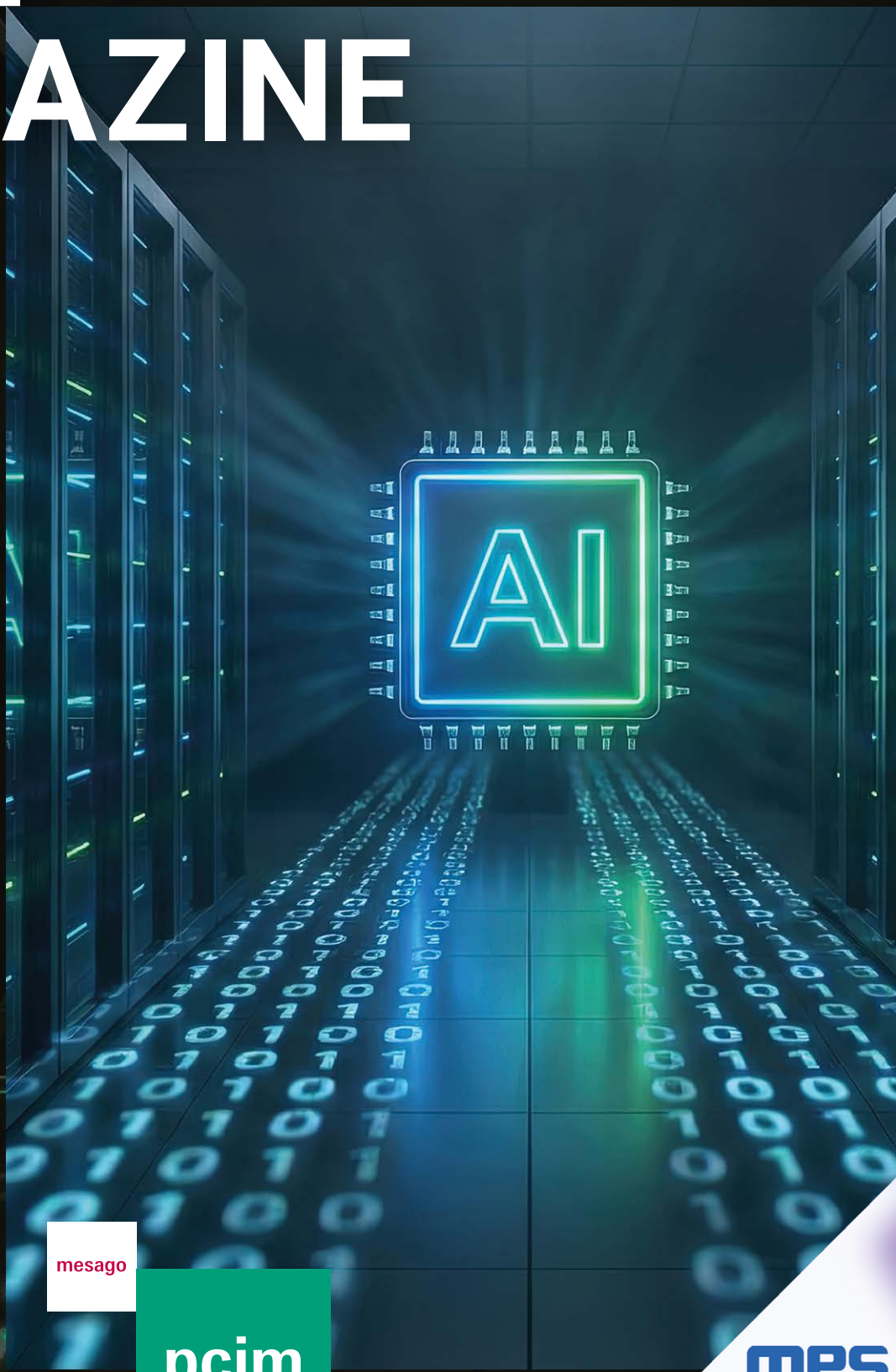

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Editorial

Never before has the energy demand of digital technologies been as high as it is today. With the rapid growth of AI applications, data centers are reaching entirely new power levels – from tens of kilowatts per rack to the megawatt class. This makes one thing clear: it is no longer computing power alone that determines the progress of AI, but above all the ability to provide and manage energy efficiently.

This year's Event Edition explores this transformation from different perspectives. Companies such as Infineon Technologies, STMicroelectronics, and Nexperia present various approaches – from megawatt server racks and 800 V DC architectures to the energy infrastructure as a limiting factor, and SiC-based solutions for more efficient and sustainable data centers.

That these developments are no coincidence, but the result of decades of innovation, is illustrated by the contribution of Prof. Leo Lorenz. From the first power diodes and thyristors to MOSFETs and IGBTs and up to SiC and GaN, he traces the evolution of power semiconductors and captures their significance in a clear message: power semiconductors are far more than just components; they are among the key enabling technologies of modern electrification.

A look into the future of energy distribution is provided by Prof. Dražen Dujic in his contribution on Solid-State Transformers (SSTs). This technology combines a wide range of conversion concepts in highly integrated modular systems and is gaining significant industrial momentum after years of intensive research.

The articles in this issue clearly demonstrate that the future of AI will not be defined by computing power alone, but by the ability to master energy across the entire system architecture.

Enjoy the read, and the PCIM Expo & Conference!

Best Regards

Lisette Hausser
Vice President PCIM

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Peak Current Load SMD ferrites: Better Resilience against Current Peaks

Due to their multilayer structure, chip bead ferrites are sensitive to current peaks, which typically occur when switching on power supplies or electric motors. However, an optimized layer design improves their resistance to short-term high current surges.

By Markus Holzbrecher, responsible developer / product manager for EMC ferrites for PCB assembly and Mohamed Koobar, responsible developer/product manager for EMC ferrites, both Würth Elektronik eiSos.

A chip bead ferrite is an inductor that is manufactured using a screen-printing process and is typically used in EMC filtering. The component consists of a nickel-zinc ferrite and has an inner silver conductor layer a few micrometers thick. This structure makes the classic SMD ferrite susceptible to current peaks above the maximum rated current. These can lead to damage or immediate destruction of the component. The following therefore applies to SMD ferrites in general, where the maximum rated current in the data sheet also defines the largest permissible current amplitude for short-term loading.

With the WE-MPSB component series, however, multilayer ferrites are available, whose data sheets offer a separate peak current consideration. Würth Elektronik has developed an optimized layer design for these products with the aim of achieving high currents, a DC resistance RDC reduced by up to 75 percent and the highest possible impedance over the entire frequency spectrum.

Figure 1 shows a typical application: The multilayer ferrite at the input of the circuit is used as a inline filter. At the moment of switch-on, a very high pulse current flows briefly due to the low ESR of the capacitor. This briefly loads the SMD ferrite with a multiple of the specified maximum rated current. In this example, the optimized multilayer ferrite, which Würth Elektronik refers to as a “multilayer power suppression bead”, or MPSB for short [1], has an impedance of 600Ω with a maximum permissible rated current load of 2.1 A. The single current peak in this circuit reaches a value of approx. 19 A, and it lasts for 0.8 ms before it decays to the rated current of the circuit.

For SMD ferrites, the maximum rated current generally defines the maximum current amplitude under short-term load. Multilayer ferrites are available in the WE-MPSB series with pulse load, which considers the peak current in the data sheet.

Test procedure for pulse load capacity

Current peaks often occur, for example, during turn-on of various switching power supplies and electric motors. Well-known applications with recurring pulses are, intermittent windshield wiper motors in vehicles, or ballasts for lamps, which can generate a high current peak at the moment the light is switched on. In particular, the input capacitor in a switching regulator often causes a high current peak, which an upstream EMC filter must withstand. In this context, pulses are understood to be short-term current peaks with a time limit of less than 8 ms until the DC current of the circuit has completely decayed.

In the search for a uniform standard for measuring the pulse load capacity of SMD ferrites, the appropriate approach was found in the definition of the melting integral for fuses. To determine the I²t value of the fuses, a pulse of 8 ms is applied to the fuse in accordance with the fuse test process, an interval long enough to heat the fuse. If the fuse holds, the current is increased further until the increase leads to the destruction of the fuse. A pause of 10 s is required between the pulses to give the component the necessary time to cool down. Würth Elektronik has developed a test routine for the multilayer ferrite based on this fuse standard. The rectangular pulse shown in Figure 2 was selected as the pulse shape for all tests because it loads the component with the highest possible energy during the pulse length, even though it will only be encountered very rarely in practice at the moment of switch-on.

Empirically measured pulse strength

In comparison to the fuse, with multilayer SMD ferrite it is not possible to specify a generally valid formula with which one can draw conclusions about the different peak currents at different pulse lengths by calculating the melting integral. The empirically determined data sheet values are based on long-term test series with different parameters.

To illustrate the inapplicability of the melting integral for multilayer ferrites, take the example of WE-MPSB article 742 792 206 01 (Z = 600Ω, IR= 2.1 A, RDC,typ= 43 mΩ), which has a maximum peak current carrying capacity of 18 A with a pulse length of 8 ms. This results in an I²t value of 2.592 A²ms (18 A @ 8 ms (5 s pause, 24°C) I²t = 2.592 A²s).

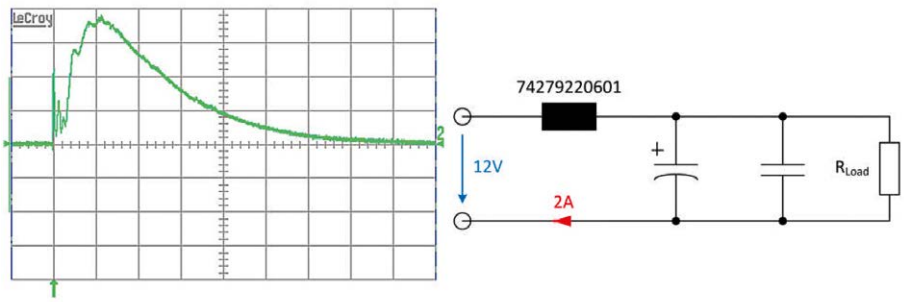

Figure 1: Typical application with peak current at switch-on (5 A/DIV | 100µs/DIV) (Image: Würth Elektronic eiSos)

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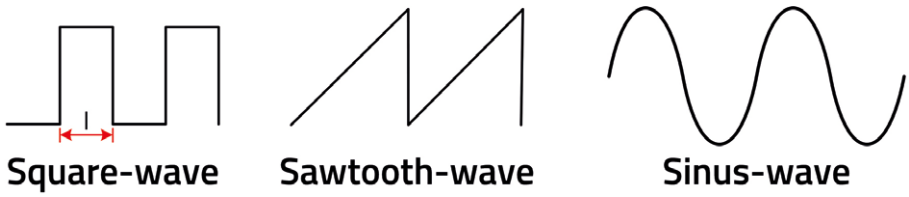


Figure 2: Possible pulse shapes at the switch-on moment. The square-wave pulse represents the highest load on the component and is therefore used in the test routine. (Image: Würth Elektronic eiSos)

If you calculate the current at a pulse length of 2 ms based on the I²t value for 8 ms, you get the following result:

$$I[A]_{@n[ms]} = \left(\sqrt{\frac{I^2[A] * 8[ms]}{n[ms]}}\right)$$

$$I[A]_{@2[ms]} = \left(\sqrt{\frac{2{,}592}{2[ms]}}\right)$$

$$I[A]_{@2[ms]} = 36\,A$$

However, the data sheet value (Fig. 3) is specified as maximum of 24 A at 2 ms. The calculated I²t value therefore deviates significantly from the measured values. Consequently, due to this deviating behavior of the SMD ferrite from fusing, it is not possible to use the known calculation of the melting integral I²t applied to a multilayer ferrite.

SMD ferrites are generally not suitable for high pulse currents due to their multilayer structure. Würth has developed an optimized layer design that handles high currents, has up to 75 percent lower RDC and the highest possible impedance across the entire frequency spectrum. Depending on the impedance and current amplitude, the optimum design is used for each individual component.

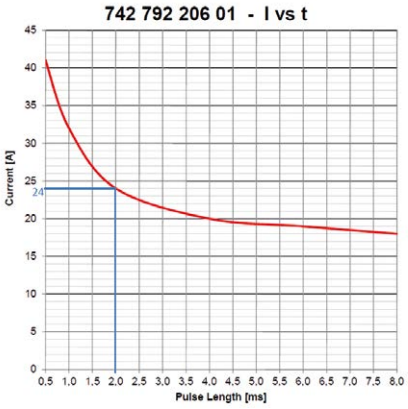


Figure 3: Specified peak current carrying capacity according to data sheet (Image: Würth Elektronic eiSos)

Using the example of four selected MPSB components, the pulse strength can be examined in more detail. The current-pulse duration curve shown on the left in Figure 4 shows the maximum permissible peak current for the respective pulse durations tested. The tested range extends from 0.5 ms to 8 ms.

The maximum permissible pulse current (Fig. 4 right) for repetitive pulses is shown in the second curve in the data sheets. This curve is a limit value consideration of the maximum peak current for repetitive pulses. A maximum pulse length of 8 ms was selected to determine the curve.

Factors influencing the pulse load capacity

The primary factors influencing the pulse load capacity of SMD ferrites are:

- The pulse length t, which is tested from 0.5 ms to 8 ms as standard. The longer the pulse, the lower the maximum pulse load capacity.
- The number of pulses, which is tested from 10 to 100,000 pulses (Fig. 4 right). As the number of pulses increases, the maximum permissible pulse load capacity decreases.
- The third reducing factor to consider is the temperature: as the temperature rises, the RDC increases, which leads to a further reduction in the maximum pulse load.

Each of these interlinked systems is subject to the dependence of the underlying pause between the individual pulses. To analyze the interlinked system with a shorter pause time, it is necessary to measure the influencing factors temperature [T], pulse repetitions [n] and pulse length [t]. The aim of the WE-MPSB series is to achieve an impedance comparable to that of the WE-CBF series. While the WE-CBF components are usually destroyed if the rated current is exceeded, the WE-MPSB components are designed to withstand higher pulse currents (Fig. 5).

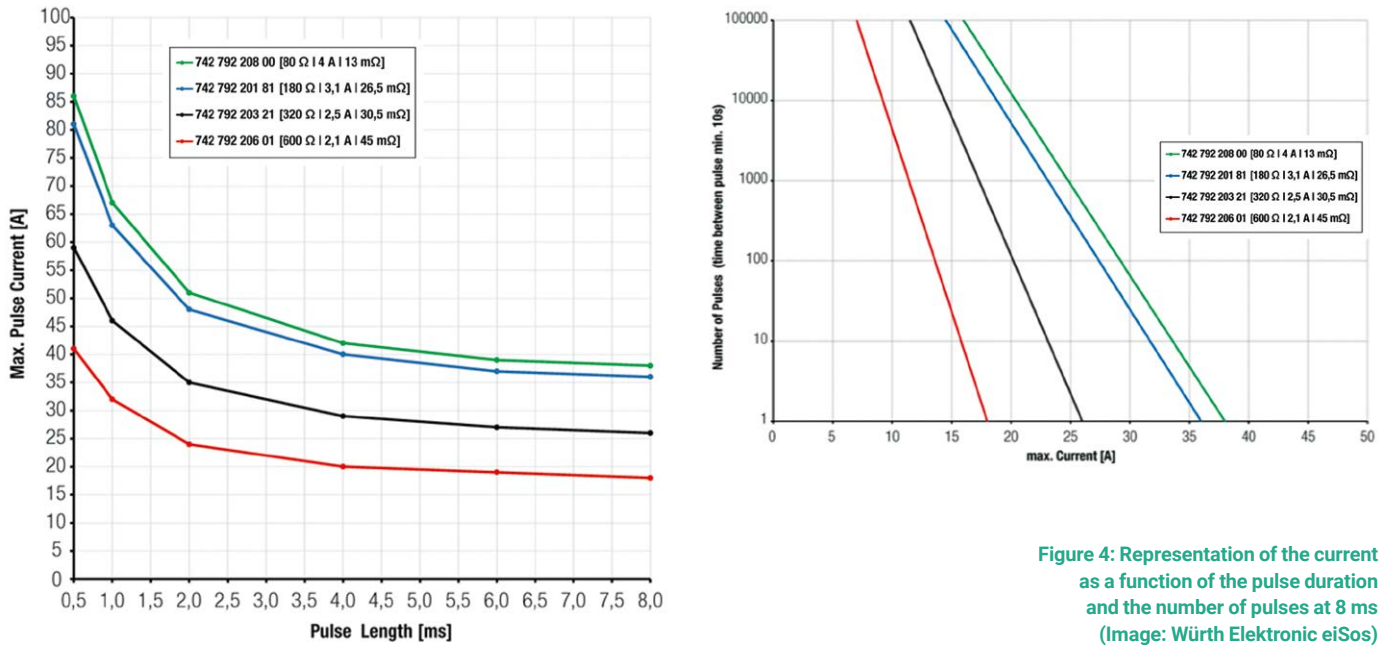


Figure 4: Representation of the current as a function of the pulse duration and the number of pulses at 8 ms (Image: Würth Elektronic eiSos)

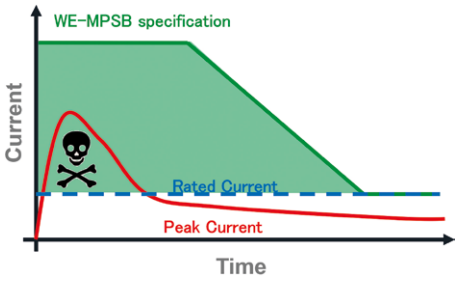


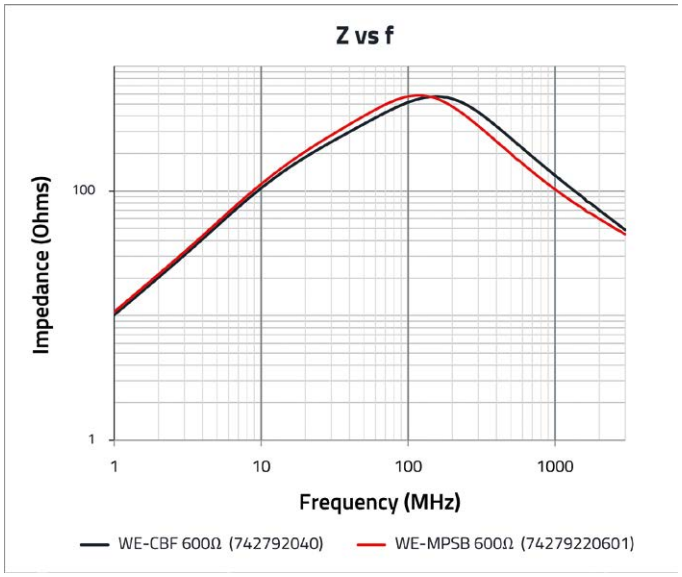
Figure 5: The WE-MPSB series is designed for a higher pulse current carrying capacity and thus withstands current peaks that occur during the switch-on process. (Image: Würth Elektronic eiSos)

Using the example of the 600Ω types in size 0805 shown in Figure 6, the WE-MPSB series has a higher rated current due to the lower resistance.

The WE-MPSB series has a significantly higher pulse load capacity than a comparable component of the WE-CBF series. Figure 7 shows the maximum pulse height of the WE-CBF 600Ω type on the left and the maximum pulse height of the comparable WE-MPSB 600 Ω type on the right. The WE-MPSB series was developed based on the requirements of circuits that load the multilayer ferrites with short-term peak currents in excess of the rated current. Compared to existing multilayer structures, the layer structure has been optimized to achieve a higher current carrying capacity through lower resistances. This makes the WE-MPSB series particularly suitable for use in circuits with pulse currents.

Wide range of components

The WE-MPSB family includes components with an impedance Z (at 100 MHz) of 8 Ω to 600 Ω in sizes 0603 to 3312 (Fig. 8). The permissible peak inrush current IR is 2.1 A to 10.5 A, depending on the component. The direct current resistance RDC ranges between 1.0 mΩ and 80 mΩ. The specified frequency range extends from 1 GHz to 3 GHz. Qualification for an extension of the frequency range up to 8 GHz is currently being carried out.



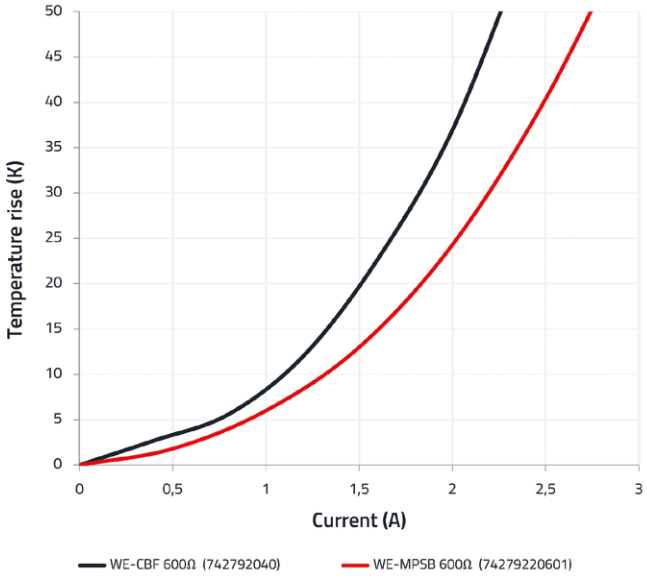


Figure 6: Comparison of the impedance and rated current carrying capacity of the WE-CBF and WE-MPSB 600 Ω type (Image: Würth Elektronic eiSos)

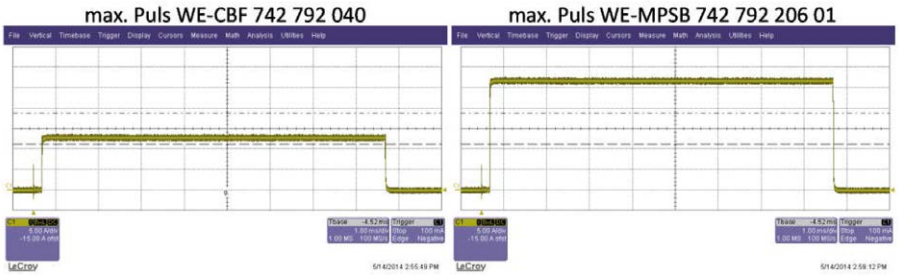


Figure 7: Comparison of the pulse load capacity of the WE-CBF and WE-MPSB series (Image: Würth Elektronic eiSos)

For currents above 5 A, the PCB layout plays an increasingly important role with regard to the current carrying capacity of the conductor tracks. Würth Elektronik is therefore currently working on design tips for this. eg

Figure 8: The WE-MPSB family comprises components in sizes 0603 to 3312 (Image: Würth Elektronic eiSos)

AI Data Centers: The Radical Shift from 480-VAC to 800-VDC Architectures

In light of the immense increase in power consumption for data centers, the transition is underway from the traditional 480-VAC architecture in data centers to 800-V architectures, which promise significantly more efficient energy use in the future.

First, the facts: According to the International Energy Agency (IEA), the global energy demand of data centers currently stands at approximately 500 terawatt-hours (TWh) per year. In total, this corresponds to roughly 1.5 to 2 percent of global electricity consumption. To put this into perspective: 500 TWh/year is more than Germany's total annual electricity consumption.

And the trend is clear: global electricity consumption is growing steadily. According to the IEA, in 2025 alone, the energy demand of data centers worldwide rose by about 17 percent. Against this backdrop, international market research firms such as Gartner predict that global electricity consumption is highly likely to double to over 900 TWh by 2030. The IEA estimates a figure of around 945 TWh.

Looking at the global distribution of data center electricity consumption, the Canadian data analysis and forecasting firm Incorrys concludes that the lion's share of global data center electricity consumption is accounted for by the U.S. and China—together nearly 70 percent. IEA figures, which still refer to 2024, put the U.S. share at 45 percent and China's at 25 percent. Europe's share in this area stood at 15 percent at that time.

The dynamic nature of developments in recent years is evident from the fact that the average annual growth in electricity consumption in the data center industry has been around 12 percent since 2017. This means that growth in this segment is four times higher than the general global increase in electricity demand. Given the global hype surrounding AI, current growth rates are unlikely to remain at these levels. The IEA therefore currently expects global electricity consumption to reach around 1,200 TWh by 2035.

If 100 percent of the electricity used were converted into "computing power," that might still be acceptable. But even modern data centers have an average Power Usage Effectiveness (PUE) of only 1.3 to 1.5. Specifically, this means that between 25 and 35 percent of the total energy consumed is lost as waste heat. This waste heat is primarily generated by the cooling required for the facility and the uninterruptible power supplies (UPS) needed to compensate for power fluctuations and outages. Modern Hyperscale data centers operated by major cloud providers currently achieve PUE values of 1.1 to 1.2, setting the standard for best practices.

The boom in energy-intensive AI processors is gradually pushing traditional cooling technology to its limits, as the use of AI chips generates a great deal of heat in a very confined space. Switching to more efficient water cooling would be one way to address the waste heat problem, or tackling the issue more radically by changing the system architecture in data centers. So far, these centers have relied on 480-V AC architectures and primarily silicon-based semiconductors. Increasing the supply voltage would enable the transmission of high power with lower losses. This would, on the one hand, reduce the weight of the required cabling and, on the other, avert the looming thermal overload.

In concrete terms, this means that in 800-V DC systems, less current flows at the same power output due to the higher voltage. Since losses are known to increase quadratically with current, waste heat is significantly reduced. To operate as efficiently as possible with the required power electronics, the era of AI has finally ushered in the age of wide-bandgap components such as SiC and GaN in modern data centers. Manufacturers have already gained experience with 800-V systems in recent years in the e-mobility sector, where 800-V architectures have also been making waves in terms of efficiency and power for a relatively short time.

As a technology leader in the AI sector, Nvidia demonstrated nearly two years ago how the challenges associated with 480 VAC at the architectural level and the 54-V standard at the rack level can be resolved. Currently, data centers perform AC-to-AC conversions in several steps before the power is converted to direct current in the server rack. In the future, there will be only a single AC-to-800-V DC conversion. This 800 VDC will then be distributed within the data center and used directly by the server racks.

To bring this project to fruition, Nvidia is collaborating with nearly 30 partners worldwide, including plant engineering firms such as ABB, Schneider Electric, and Siemens, as well as gas turbine manufacturers like GE Vernova. However, the majority of these partners are semiconductor specialists such as Analog Devices, EPC, Infineon Technologies, Innoscience, Mitsubishi Electric, MPS, Navitas, onsemi, Power Integration, Renesas, Rohm Semiconductor, STMicroelectronics, and Texas Instruments.

The following articles from Infineon Technologies, Nexperia, and STMicroelectronics, for example, illustrate how power semiconductor specialists are specifically adapting to the new era of 800-V data centers and what benefits their products offer for the AI boom. eg

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The path to megawatt server racks and DC microgrids

Artificial intelligence presents new challenges for data center operations. In particular, power supply and distribution must be completely reinvented to meet growing demands. How can switching to 800 V DC supply voltages help?

By Sam Abdel-Rahman, Senior Principal System Architect at Infineon Technologies

Image: zhou yan/stock.adobe.com

Artificial intelligence (AI) is playing an increasingly important role in countless fields of application. Providers are expanding their data centers to meet this growing demand. More specifically, training ever-larger AI models requires increasingly powerful computing capabilities, including the clustering of up to 100,000 processors into a single virtual machine.

These growing demands are also creating new challenges in power supply at every level – from individual processors to entire data centers. Modern processors need to operate at ever higher load currents and handle strong transient load steps. Power requirements are expected to reach up to 10,000 A per processor within this decade, representing a tenfold increase compared to requirements seen today. AI server racks will require power levels beyond 1 MW. This again represents a tenfold increase in rack power compared to the current standard. Entire data centers will reach power levels in the gigawatt scale, which will necessitate a different infrastructure and new ways of power distribution within the data center. Furthermore, as data centers are turning into substantial consumers of electricity, buffering of load profiles and providing ancillary grid services will become essential.

In addition to these requirements, the power supply for AI data centers must be designed to be as efficient as possible in order to conserve energy despite this enormous energy demand, especially in the face of climate change. Driven by the rising power draw of modern GPUs and the need to cluster more of them per rack, it is clear that traditional power distribution architectures will struggle to support gigawatt-scale data centers without a fundamental redesign. Just as semiconductors have always enabled data processing, storage, and transmission at the heart of data centers, they will also play an increasingly important role in power supply systems in the future. With their help, high power density and efficiency can be combined.

DC microgrids

Achieving ultimate efficiency in an AI data center requires a holistic optimization of the entire power distribution, from energy generation to consumption. As the power demand approaches the gigawatt scale, a new infrastructure for power distribution is required to optimize energy efficiency and, consequently, operational expenditure. DC microgrids are the most likely solution to shape the future of AI data centers. They represent a rethinking of how power is managed within the infrastructure of data centers.

In today's 48-V architecture, the server racks are powered by AC voltage, with AC/DC conversion taking place individually in each rack. Centralized power generation directly from the MV AC grid (10 to 35 kV AC) and distribution via high-voltage DC removes these AC-DC power supplies from the power flow. Thus, within the server rack, only DC-to-DC conversion is required, allowing more efficient and

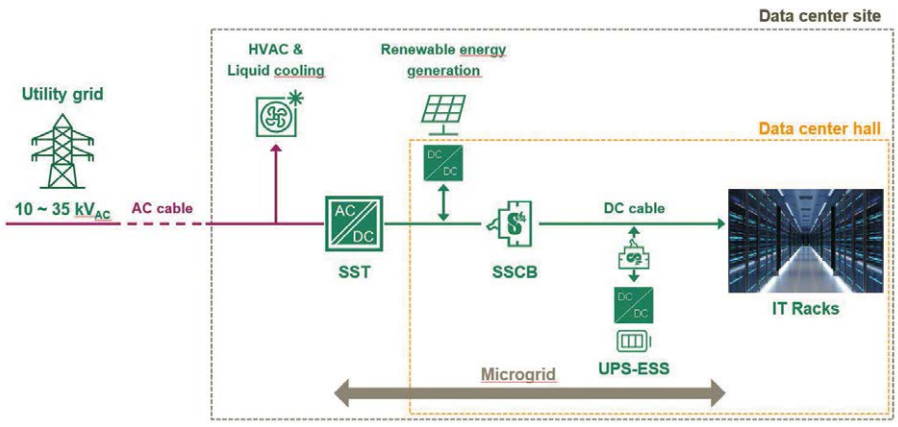

Figure 1: Architectural changes of the power flow for evolving energy demands of AI data centers. Infineon power semiconductor solutions drive efficiency in every power stage, no matter whether it is DC-DC, AC-DC, or DC-AC (Image: Infineon Technologies).

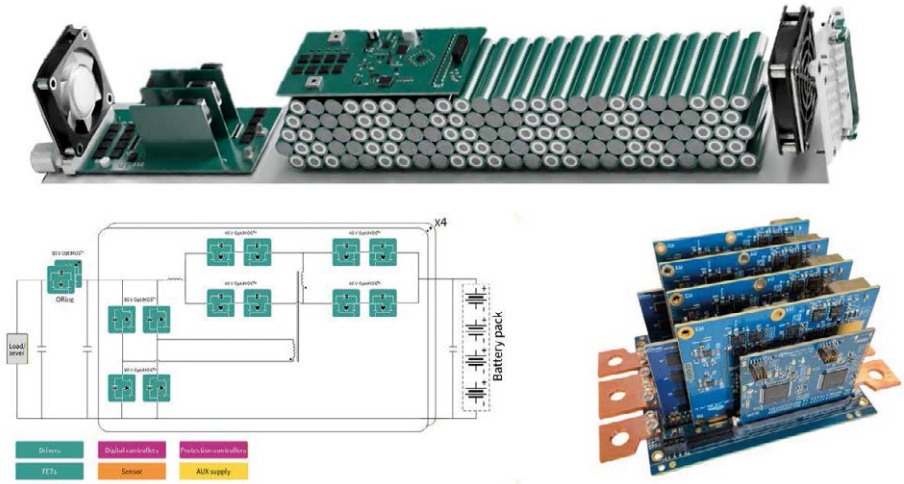

Figure 2: A sample circuit for a 12 kW BBU (Image: Infineon Technologies).

more compact power conversion that may be integrated at the server board level, as outlined above. The DC microgrid becomes the central infrastructure element of the data center, providing energy on an HV DC bus to the server racks as a future-proof scalable solution. Figure 1 illustrates such a scenario.

SSTs and SSCBs: Semiconductors for DC microgrids

In such a scenario, the emerging technology of solid-state transformers (SSTs) will play a decisive role. SSTs are capable of receiving power from the MV AC grid at voltage levels of 10 kV AC to 35 kV AC and providing a regulated high-voltage DC distribution required by the server racks. Their relative compactness and lower weight in comparison to conventional MV transformers allow them to be placed close to server racks for minimal transmission losses. SSTs are expected to provide 2 to 10 MW of power per unit, offering benefits in efficiency, power density, and scalability.

An SST is typically built as an Input-Serial/Output-Parallel (ISOP) system, in which multiple series-connected converter cells form a string that is connected to each phase of the MV Grid. MV AC grid voltages are country-specific and may range from 10 kV AC to 35 kV AC. The SST provides a rectification stage and an isolated DC-DC stage, with all outputs feeding into one DC bus at, for example, 800 V DC. Each converter cell may use either 2-level or 3-level topologies. Infineon supports these applications with a broad portfolio of CoolSiC MOSFETs and IGBTs covering voltage classes from 750 V up to 3300 V. Especially the high-voltage class devices will reduce the complexity of the SST system by decreasing the number of required subsystems.

SSTs provide voltage regulation and disconnect options from the grid in case of failures. Downstream solid-state circuit breakers (SSCB) will be key elements for safety and reliability. With their fast turn-off capabilities, failures can be isolated at relatively low fault currents. CoolSiC JFET devices will be the technology of choice for these tasks. Combining SSTs with SSCBs and subsequent DC-DC stages enables a fully semiconductor-based power conversion chain from grid to core.

Distributed Energy Resources

A further advantage of the DC microgrid architecture is the ability to directly couple distributed energy resources (DERs). These diverse power sources, such as solar, fuel cells, or batteries, can be connected on a high-voltage DC level without any DC-to-AC and AC-to-DC power conversion. Further auxiliary systems, such as HVAC and chillers for liquid cooling, could also be adapted to a DC input and reduce losses due to minimizing the number of power conversion stages.

BBUs: Battery Backup Units

Batteries, in particular, are highly beneficial in AI environments, as they can bridge power outages and cushion consumption spikes caused by intensive computations without placing additional strain on the grid. A battery backup unit (BBU) is used for this purpose, which is composed of a battery management system (BMS) and a DC-DC converter. The BMS allows safe and high-performance operation of Li-ion batteries. It is essential and performs state-of-charge (SOC) and state-of-health (SOH) estimations. The BMS circuit is coupled with a DC-DC converter to provide a regulated output voltage (Figure 2).

For these applications, Infineon offers suitable DC-DC converters, with high power density, efficiency, and thermal performance in the same form factor as today's low voltage BBUs. This is enabled by 650 V/1200 V SiC technology. Built around a multi-level, multiphase architecture, they cut magnetic volume through stacked, interleaved, and coupled non-isolated Boost (discharger) and Buck (charger) stages, converting directly from a battery stack to an 800 V DC bus.

PSUs: From 48 V to high-voltage DC

In today's era of pre-DC-microgrids, 48-V DC power has become the standard. With the rising power consumption of modern GPUs and the need to cluster more GPUs per rack, power levels per rack will rise to 1 MW and beyond. These power levels are pushing the 48-V ecosystem past its limits, so that higher DC voltages are required here as well.

Traditionally, every rack contains power delivery components, backup power, and IT payload, leveraging single-phase power supply units (PSU) of increasing wattage. As rack power levels exceed 250 kW, the architecture is shifting towards dedicated sidecar racks for power delivery and backup power, along with a transition to three-phase AC power delivery (Figure 3). Finally, as rack power levels continue to rise, data centers are expected to adopt a fully centralized high-voltage DC power

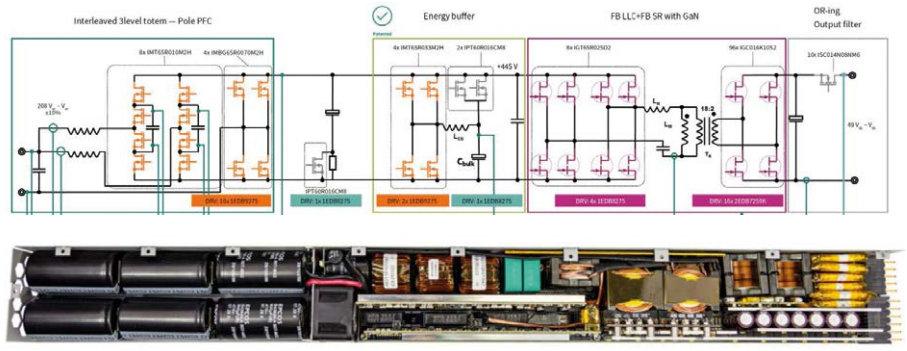

Figure 3: A 12kW 50V PSU for IT racks (Picture: Infineon Technologies).

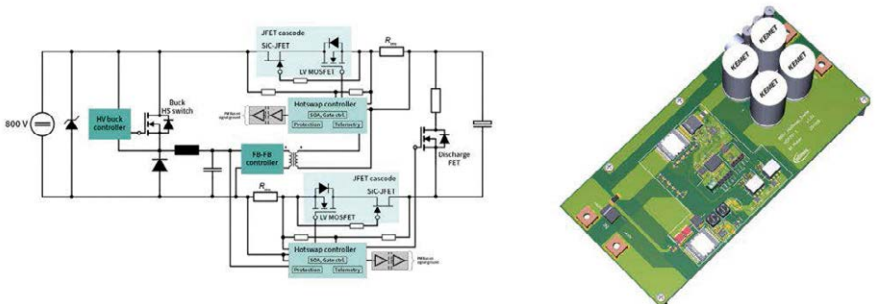

Figure 4: The hot-swap XDP711 with 6 kW from Infineon (Image: Infineon Technologies)

distribution architecture, enabling efficient power distribution across the entire facility.

eFuses and hot-swap functions

Future server boards will consequently operate directly from 800 V or ±400 V, respectively. This requires several new functions, such as pre-charging of server boards before connecting them to the HV DC bus and discharging of switches to avoid hazardous voltages when a server board is removed from the IT rack (Figure 4). In addition, eFuse functionality is required to interrupt the supply voltage in case of failures. This is an essential safety aspect, which must be implemented on every server board.

IBCs: Supplying the server board

The server board also requires a transition. Despite the high-voltage power supply in the rack, GPU supply voltages remain below 1 V. This means the voltage conversion must take place on the server board, within a space-constrained environment. This can be achieved using either a two-stage configuration via 12 V (800 V to 12 V) or a three-stage configuration of 800 V via 54 V and 12 V (800 V to 54 V to 12 V). While a three-stage approach with 800 V-to-54 V as the first stage, followed by an Intermediate Bus Converter (IBC) and VRM power stages or backside vertical modules, reduces losses in the power delivery network and supports mezzanine card solutions (with the IBC and VRM stages both being placed on the mezzanine card), a two-stage solution with 800 V-to-12 V eliminates an entire power conversion stage and may save precious space on the motherboard. IBCs, in particular, must meet high expectations in this scenario: maximizing end-to-end efficiency to limit thermal load, achieving very high power density near GPUs/XPUs, managing EMI in tightly packed systems, and accelerating design cycles despite increasing conversion complexity across multiple voltage domains (Figure 5).

From grid to core: the road ahead for AI data center power architecture

The future of AI is inextricably linked to the development of advanced power solutions. The increasing power demands of AI data centers, with server boards exceeding 10 kW, server racks surpassing 1 MW, and entire data centers approaching the gigawatt scale, pose significant technological challenges. To address these challenges, advanced semiconductor solutions are necessary to handle complex power conversion processes while improving energy efficiency, power density, robustness, and total cost of ownership. Infineon is taking a holistic approach to addressing these challenges by offering system solutions that span from the grid to the core. The development of corresponding power management solutions, including SSTs, SSCBs, IBCs, and PBUs, will be crucial for realizing high-voltage data center architectures of the future. eg

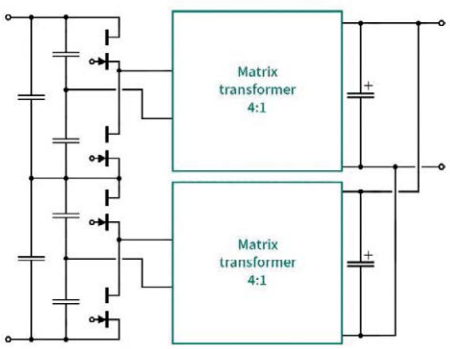

Figure 5: Example circuit of a HV IBC from 800 V to 50 V with 6kW (Image: Infineon Technologies)

Image: Grisp/stock.adobe.com

SiC MOSFETs as an Enabler for the Next Generation of AI Data Centers

The next evolutionary stage of artificial intelligence will not be limited by computing power—but by energy. As AI clusters push toward ever higher power densities, the central challenge is shifting from data processing to low-loss energy supply. This is precisely where a technological lever emerges that is often underestimated: the choice of power semiconductor.

By Ole Gerkensmeyer, Chief Strategy Officer, Nexperia

The use of SiC MOSFETs represents a fundamental break from traditional silicon architectures. The difference lies not only in incremental improvements, but in the physical properties themselves. Lower conduction losses and significantly higher switching speeds enable more efficient energy conversion, drastically reduce losses, and simultaneously shrink the overall infrastructure. What begins at the component level scales across the entire system—up to measurable megawatt-level effects.

Grid: Efficiency Begins at the Grid Connection

At the transition from the power grid to the data center, it is determined how much energy is actually usable. Conventional silicon solutions typically operate at efficiencies of 96 to 97 percent. In contrast, SiC-based systems achieve up to 98.5 to 99 percent. This difference of just a few percentage points may initially seem marginal, but it has a significant impact at megawatt-scale power levels.

In a 1 MW converter, losses drop from about 30 kW to around 12 kW. At the same time, the higher switching frequencies of SiC—up to 100 kHz—enable a drastic reduction in the size of transformers and filters. Fewer losses mean less cooling, less volume, and ultimately lower system costs.

Data Center: High Voltage Replaces Copper

The real revolution becomes evident in power distribution within the data center. While conventional 48 V architectures require currents exceeding 2000 A for 100 kW loads, an 800 V system reduces the current to approximately 125 A. This physical shift has immediate consequences: copper demand decreases by more than 90 percent. Instead of 30 to 50 kg per rack, only 3 to 8 kg are needed. In a hyperscale data center, this adds up to savings of 250 to 400 tons of copper. At the same time, conduction losses decrease by more than 80 percent. This is enabled not only by the higher voltage, but also by the efficiency

Ole Gerkensmeyer, Nexperia: "A conventional 48 V System require currents exceeding 2000 A for 100 kW loads. An 800 V System reduces that current to approximately 125 A. The copper demand decreases by more than 90 percent. Instead of 30 to 50 kg per rack, only 3 to 8 kg are needed."

and switching speed of SiC, which allows for compact and low-loss DC/DC converters with efficiencies of up to 98 percent. The result is a significantly leaner, more efficient, and more scalable power infrastructure.

Rack: Less Heat, More Computing Power

At the rack level, these effects directly impact the reality of modern AI systems. Accelerator chips generate extreme load transients and require highly dynamic power delivery. This is where SiC demonstrates its second major strength: fast switching.

Lower switching losses and higher frequencies improve power supply efficiency from around 88 percent to as much as 93–94 percent. For a 100 kW rack, this means a reduction in power loss from approximately 12 kW to 6 to 8 kW.

This difference is not just numerical—it is physically tangible: less heat dissipation, reduced cooling requirements (–20 to 30 percent), and more compact designs. At the same time, additional electrical power becomes available, which can be directly converted into computing capacity.

System: The Megawatt Effect

Across the entire energy chain, losses are nearly halved—from about 12–13 percent in conventional silicon systems to 6–8 percent with SiC.

For a data center with 100 MW of grid connection capacity, this translates into savings of 4 to 6 MW of continuous power—or 35 to 50 GWh per year. More importantly, it is not just the savings themselves that matter, but their impact: this energy becomes immediately available as additional IT power.

In practice, this corresponds to approximately 5 to 6 percent more usable computing capacity—or around 60 additional high-performance racks, without increasing the grid connection capacity.

At the same time, material usage drops dramatically: several hundred tons less copper, up to 50 percent fewer magnetic components, and significantly reduced cooling structures. These effects translate directly into lower capital expenditures and operating costs. Both CapEx and OpEx can be reduced by double-digit percentages.

Conclusion: From Component to System Advantage

The advantages of SiC—better conductivity and faster switching speed—are not isolated characteristics. They propagate along the entire energy chain and transform electrical efficiency into real system benefits: fewer losses, less material, and lower costs.

For operators of AI data centers, this represents a paradigm shift. Growth is no longer limited solely by energy availability, but increasingly by the efficiency of the deployed technology. At Nexperia, we therefore view SiC not as an option, but as a prerequisite for the next generation of scalable, cost-efficient, and sustainable data centers. eg

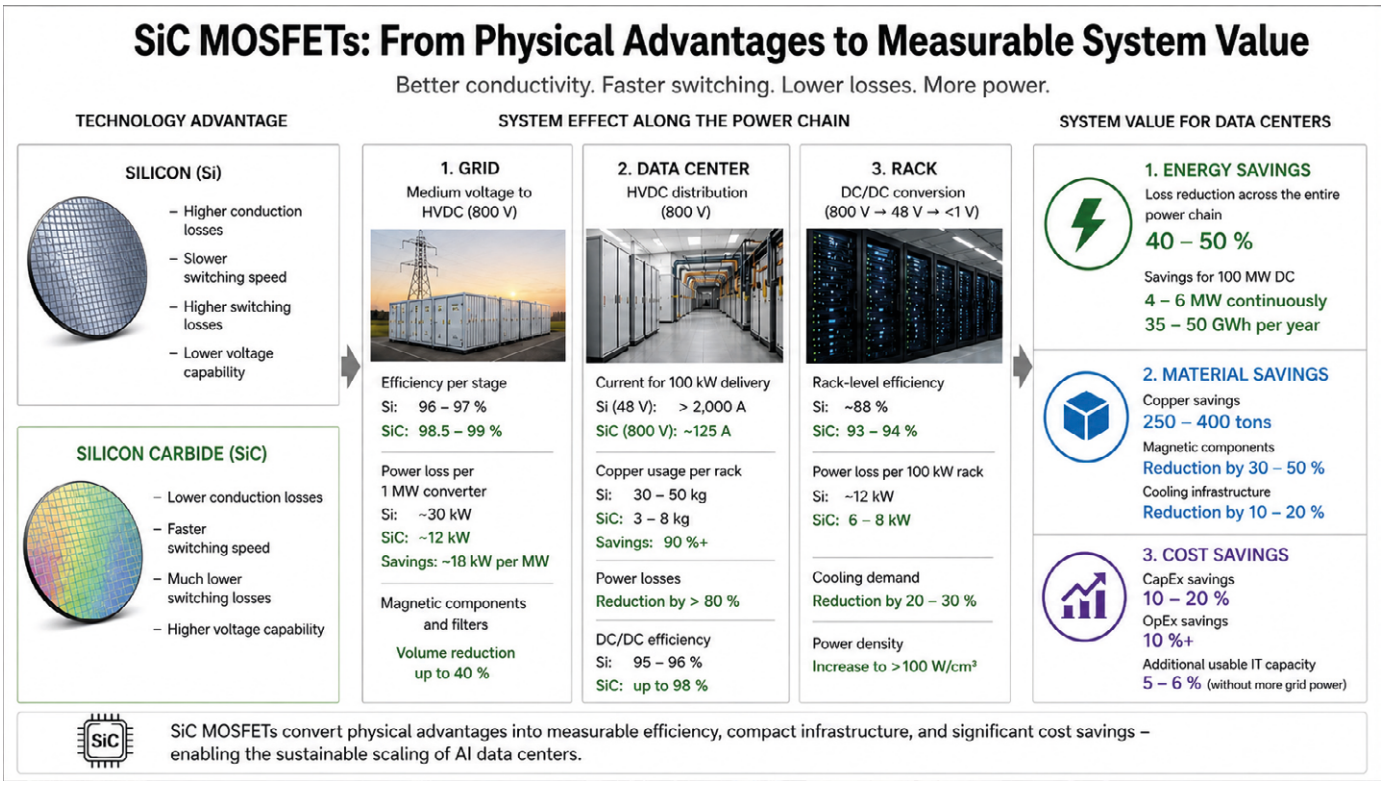

Image: Nexperia

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Why Energy Infrastructure Now Defines the Scalability of AI Data Centers

Artificial intelligence is driving an unprecedented expansion of data center compute capacity. Modern AI training and inference workloads require massive parallelism, high bandwidth memory access, and tightly coupled accelerators. As a result, AI server racks are rapidly scaling from tens of kilowatts toward hundreds of kilowatts, with emerging architectures approaching the megawatt class.

By, Mudit Srivastava – Data Center Segment Business Program Manager at STMicroelectronics

At this scale, system performance is no longer limited primarily by compute capability. Instead, power delivery, energy efficiency, and thermal management have become dominant engineering constraints. Supplying electrical energy efficiently and reliably to AI computing elements—while remaining within spatial, thermal, and sustainability limits—has emerged as a first order design challenge for data center architects. Traditional power architectures, optimized for enterprise and cloud workloads of the past, were not designed for these operating conditions. Rising currents, excessive copper usage, increasing conversion losses, and escalating cooling demands now impose fundamental physical and economic limits. Addressing these challenges requires a re architecture of how energy is distributed, converted, and managed within AI data centers.

AI Rests on Physical Infrastructure: Energy Comes First

AI is often framed as a software or algorithmic breakthrough, but its scalability ultimately depends on physical infrastructure. Every AI workload consumes energy—whether during large scale model training in hyperscale data centers or real time inference across distributed edge systems. As model complexity increases and deployment expands, cumulative power demand grows rapidly. In both centralized and distributed environments, inefficiencies in power conversion translate directly into heat, cooling overhead, and higher total cost of ownership.

Beyond computation itself, an AI data center is fundamentally defined by the interaction

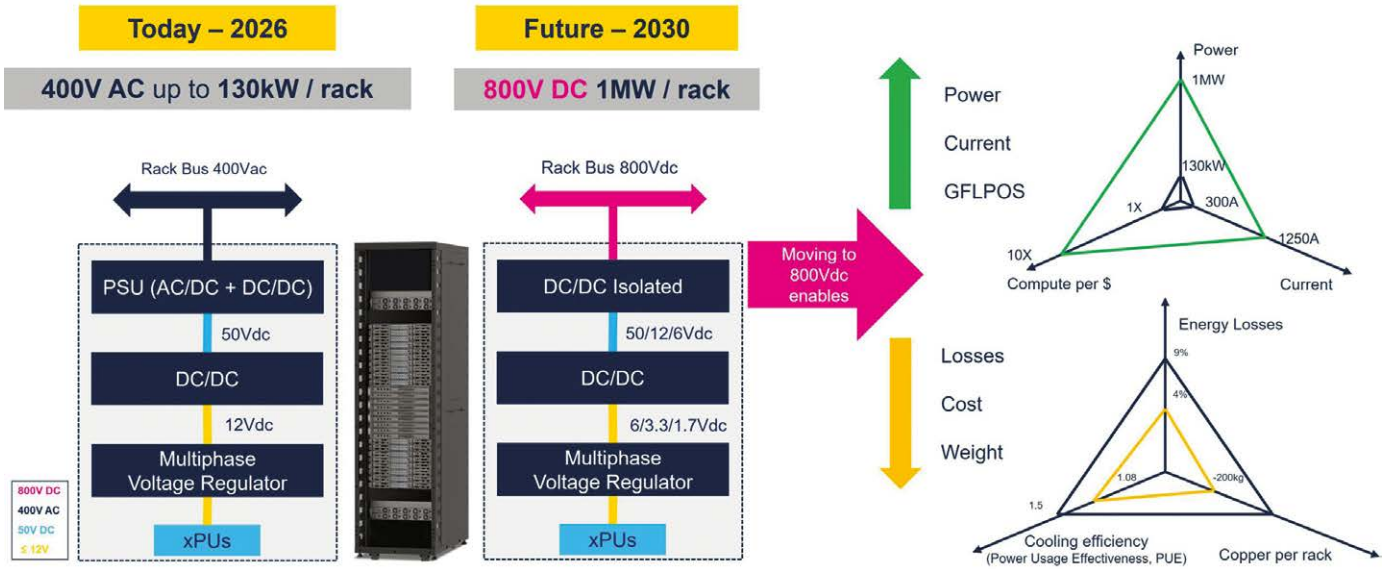

Figure 1: Transition to 800V High-Voltage DC Architecture to sustain Higher GPU Computation (Image: STMicroelectronics)

of three tightly coupled system flows: power flow, thermal flow, and network flow. Power flow concerns how electrical energy is sourced, converted, and delivered to increasingly dense compute elements. Thermal flow governs how the resulting heat is extracted and controlled as rack power levels rise. Network flow enables the massive, low latency data exchange required to interconnect large numbers of processing units into unified AI systems. These flows are interdependent and must evolve coherently as AI infrastructures scale. Energy efficiency therefore becomes inseparable from performance. Losses in power delivery do not simply waste electricity; they limit usable compute density, constrain system scaling, and increase infrastructure cost, while directly influencing thermal behavior and cooling requirements. For this reason, this article places a particular focus on power flow, examining power architectures and power semiconductor technologies as a concrete entry point into the broader engineering challenges of AI data centers—while acknowledging the essential roles of thermal management and high speed connectivity in enabling scalable AI infrastructure, domains in which STMicroelectronics acts as a technology and system level enabler.

The Limits of Low Voltage Power Distribution

For decades, data centers have relied on low voltage DC distribution, typically based on 48–54 V buses. While effective for traditional server workloads, this approach breaks down as rack power increases substantially.

Delivering hundreds of kilowatts at low voltage requires extremely high currents, leading to several compounding challenges: Large copper busbars and cabling volumes, High resistive losses and reduced efficiency, Severe thermal stress and cooling complexity, Practical limits on rack scalability.

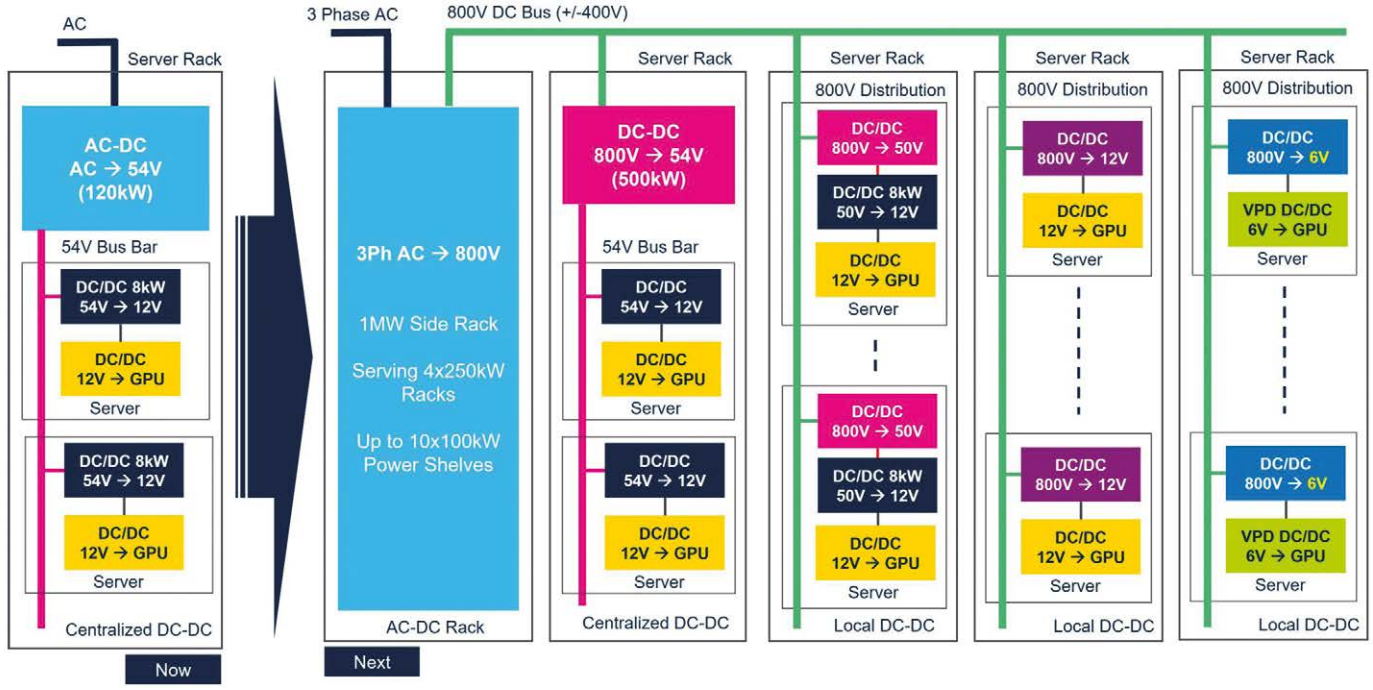

Figure 2: 800V AI Rack Power Delivery Evolution with centralized vs. localized 800 V DC-DC conversion (Image: STMicroelectronics)

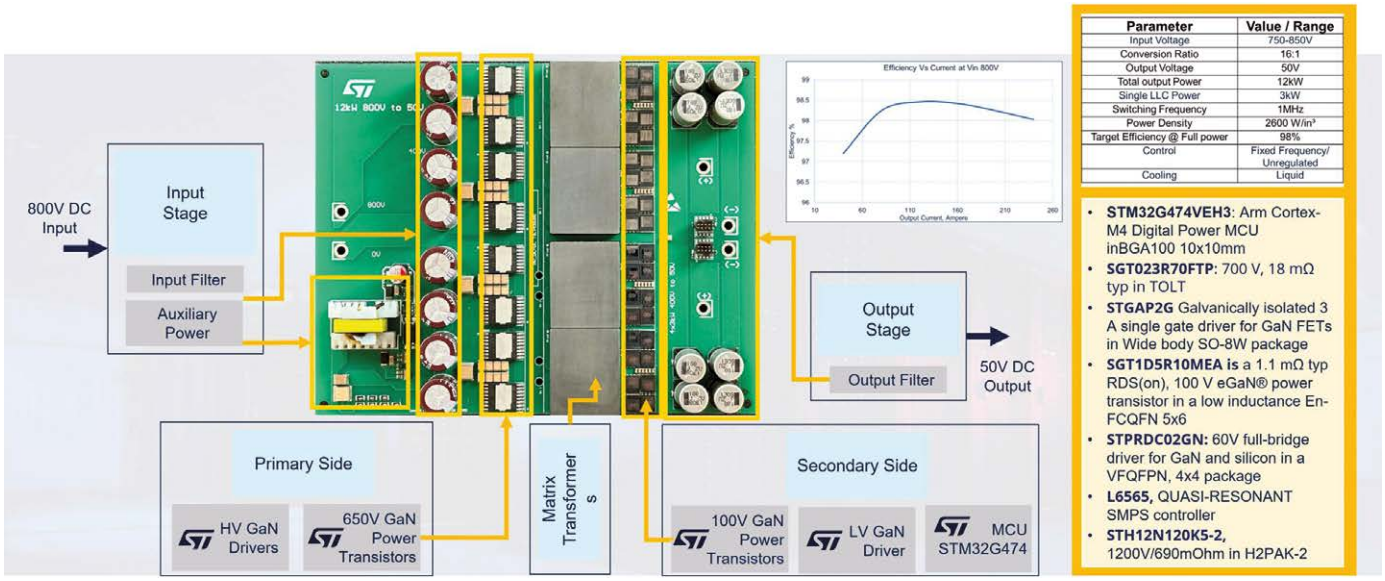

Figure 3: 12 kW HVDC 800 V to 50 V Converter (Image: STMicroelectronics)

These issues are not incremental problems; they represent fundamental physical constraints. Simply increasing conductor size or airflow cannot provide a sustainable path forward for AI scale computing.

High Voltage DC Architectures Enable AI Scalability

To overcome these limitations, next generation AI data centers are transitioning toward high voltage DC distribution architectures, in which power is delivered to racks at several hundred volts.

Raising distribution voltage dramatically reduces current for a given power level. An 800 V DC architecture, for example, reduces current by more than an order of magnitude compared with a 54 V system.

Figure 1 illustrates how this architectural shift yields immediate system level benefits:

- Lower conduction losses
- Significant reduction in copper usage
- Improved overall energy efficiency
- Greater flexibility for rack level scaling
- Simplified thermal management

In such architectures, AC to DC conversion is typically centralized upstream, while high voltage DC is distributed directly to the racks. Inside the rack, power is then converted to intermediate and point of load voltages required by processors, accelerators, and memory subsystems.

Rack Level Conversion: Centralized vs. Localized Approaches

Once high voltage DC reaches the rack, designers must determine how best to convert it to lower voltages. Two architectural approaches are commonly considered, as shown in Figure 2.

In a centralized conversion approach, a rack level DC DC stage generates a low voltage bus that feeds all servers. This simplifies integration but still requires substantial low voltage distribution infrastructure.

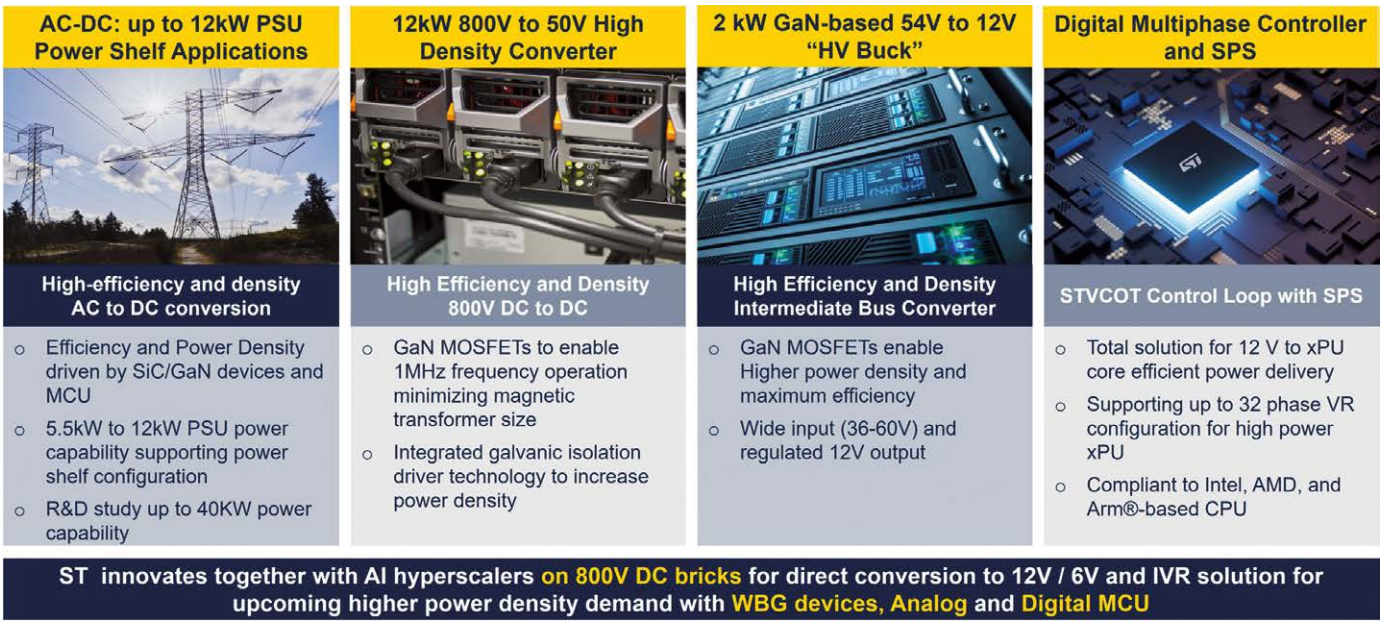

Figure 4: AI Data Center power flow system coverage (Image: STMicroelectronics)

In a localized conversion approach, the high voltage DC bus is delivered directly into each server, where it is converted locally. This minimizes low voltage distribution losses and improves scalability, but places extremely demanding requirements on power density, efficiency, and thermal performance of each conversion module.

Localized conversion is increasingly favored for AI workloads, provided that sufficiently compact and efficient DC DC solutions can be realized.

Power Semiconductors Enable High Density Conversion

Achieving efficient, compact conversion at these power levels depends critically on power semiconductor technology. Wide bandgap devices, particularly gallium nitride (GaN), enable higher switching frequencies with lower losses than conventional silicon devices.

High frequency operation allows smaller magnetic components and higher integration density, both essential for localized conversion. Resonant topologies such as LLC converters are especially attractive due to their soft switching properties and high efficiency. However, operating at high voltage, high frequency, and high power simultaneously introduces challenges in electromagnetic compatibility, thermal management, and magnetic design.

Figure 3 illustrates a representative high voltage, high frequency DC DC architecture, targeting high density localized 800 V to 50 V DC DC conversion module, highlighting the integration of wide bandgap devices, planar magnetics, and liquid cooling required to reach power densities beyond 2600 W/in³

Beyond the initial 800 V to 50 V conversion stage, high voltage DC data center architectures increasingly rely on a portfolio of downstream conversion paths optimized for different server form factors, GPU generations, and thermal envelopes. In response to this diversification, STMicroelectronics has expanded its 800 VDC AI data center power conversion portfolio to include direct 12 V and 6 V architectures, complementing the intermediate 50 V stage and allowing power delivery to move closer to advanced processors. These additional voltage domains reduce the number of conversion stages, limit copper usage, and improve electrical and thermal efficiency at both rack and server levels.

This portfolio approach has been developed in collaboration with Nvidia, aligned with emerging 800 VDC reference architectures for next generation AI infrastructure.

These solutions establish a coherent end to end power delivery portfolio spanning multiple voltage domains required in gigawatt scale compute environments, leveraging ST's power, analog, and mixed signal technologies with custom optimization at both chip and package levels.

System Level Optimization Beyond Individual Devices

At megawatt scale rack power, optimization cannot be performed at the component level alone. Power devices, drivers, controllers, magnetics, cooling systems, and mechanical integration are tightly coupled. Improvements in one area affect losses, temperatures, and reliability in others.

Moreover, practical considerations such as manufacturability, serviceability, sustainability, and recyclability increasingly shape architecture decisions. AI data center power systems must scale reliably over long operational lifetimes while aligning with environmental and regulatory requirements.

This reality necessitates a system level approach to power electronics, in which semiconductor technologies are designed and deployed with full awareness of their role in the complete energy chain.

STMicroelectronics' Role in AI Data Center Power Flow

STMicroelectronics addresses these challenges by enabling high efficiency power conversion across key voltage domains of the AI data center—from high voltage DC distribution to tightly regulated processor supply rails.

ST's portfolio combines:

- Wide bandgap and advanced silicon power devices for high voltage and high frequency operation
- Gate drivers, digital and analog controllers supporting regulation, protection, and telemetry
- Device technologies optimized for thermal robustness and long term reliability

Together, these elements support compact, high density DC DC conversion modules capable of delivering high power with minimal losses. By reducing conversion inefficiencies, ST solutions directly lower thermal load, simplify cooling, and enable higher compute density per rack.

As a result, future power architecture is moving toward HVDC and Solid-State Transformer (SST). Every power conversion step saved from the grid to the processing units increases efficiency and power delivery.

Figure 4 summarizes how these technologies fit within the AI data center power flow—from grid interface through rack level distribution to point of load conversion.

Beyond Data Centers: A Broader Electrified AI Ecosystem

The energy challenges driving data center power innovation are not unique. Similar constraints appear across electric vehicles, industrial automation, robotics, and intelligent infrastructure. In each case, AI increases power demand while space, weight, and cooling margins remain constrained.

Technologies developed for AI data center power—wide bandgap semiconductors, advanced packaging, and system level energy optimization—therefore form the foundation for a much broader wave of AI driven electrification across industry and mobility.

Conclusion: No Efficient Energy, No Scalable AI

AI data centers are rapidly approaching the physical limits of power delivery and thermal management. Without a shift toward more efficient, higher voltage, and better integrated energy architectures, AI scalability will be constrained by energy rather than computation.

Power semiconductors define these limits. They determine conversion efficiency, heat generation, system size, and reliability. Continued innovation in power electronics is therefore essential to enable sustainable AI infrastructure.

Ultimately, AI is only as scalable as the energy systems that support it. Without sustainable and efficient energy usage, AI will not work. With it, energy becomes a catalyst—enabling the next generation of intelligent, electrified systems. eg

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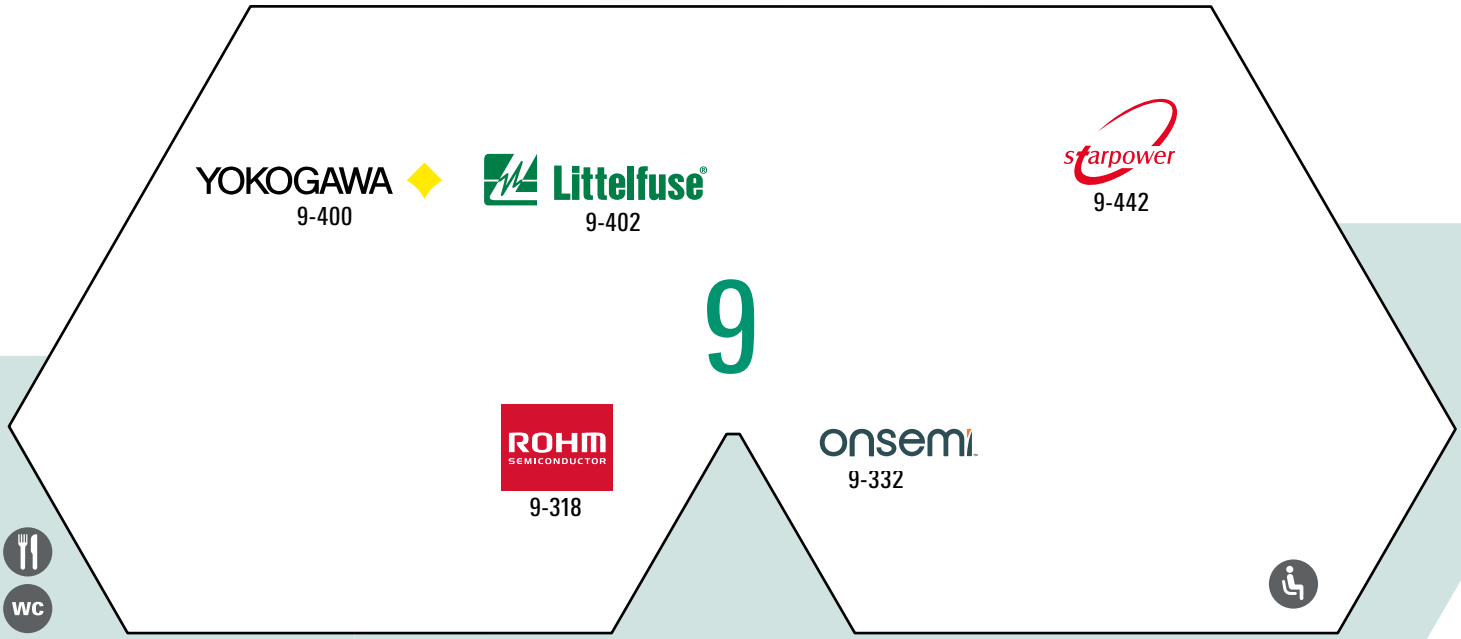
- Barrier-free WC
- Water dispenser
- ATM
- First aid post
- Parking
- Taxi
- Subway
- Security Control Unit



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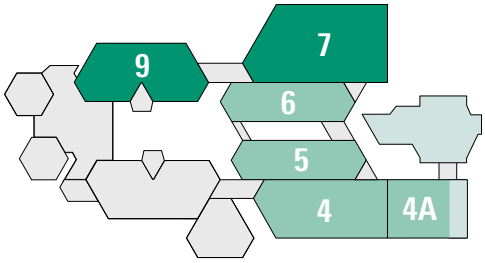

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- Robert Bosch (7-443)
- Infineon (7-470)
- Asahi Kasei Microdevices (7-502)
- Wolfspeed (7-540)
- Trio Metal (7-629)
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- First aid post
- Parking
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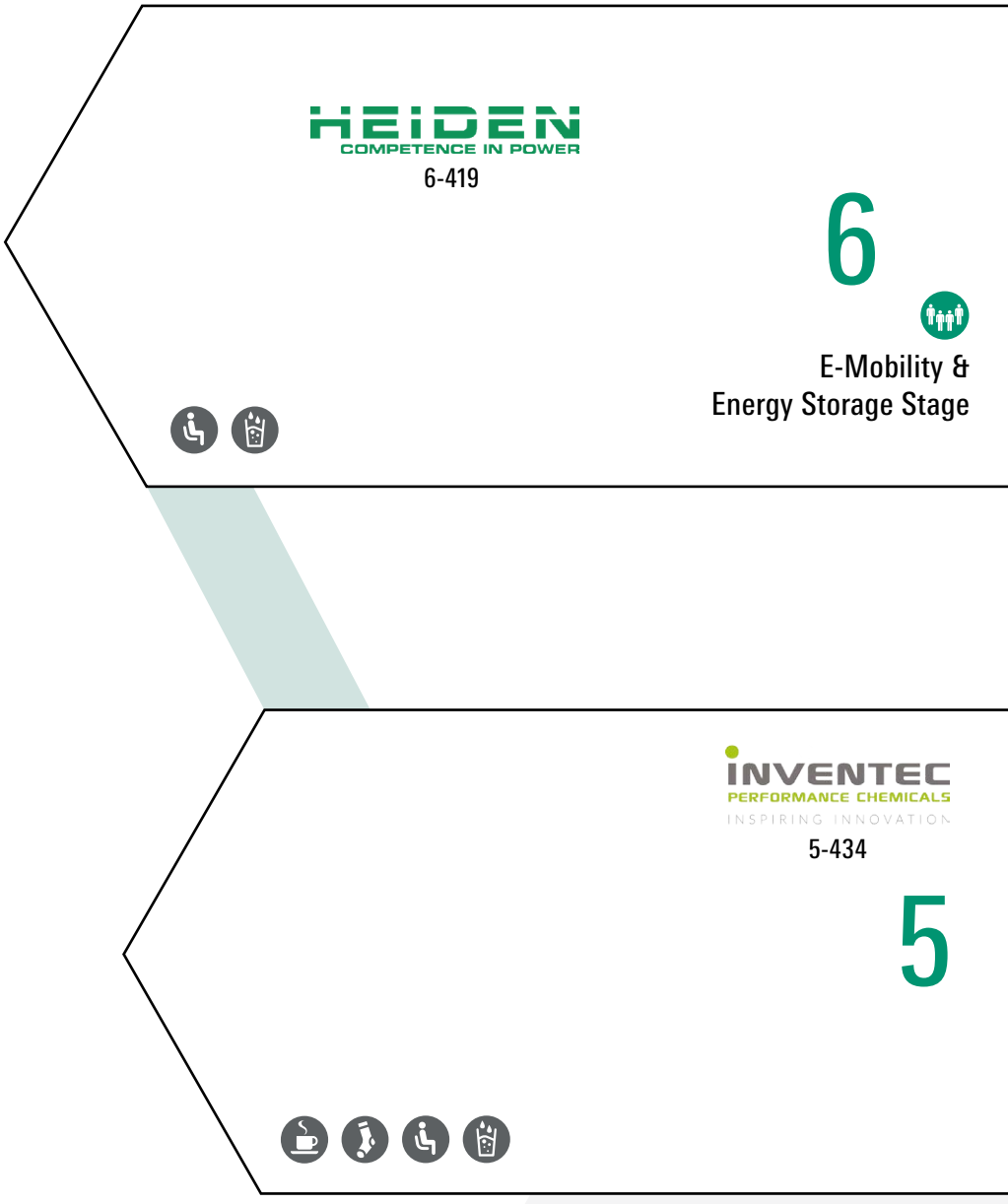
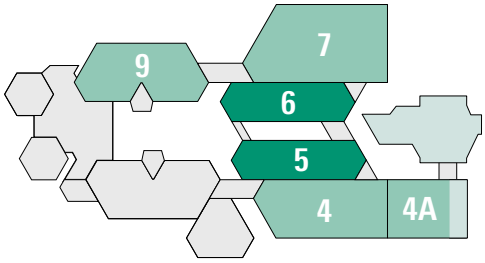
- Security Control Unit
- Press center





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- NXP Semiconductors (5-442)

Hall 6

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- Fraunhofer IZM (6-260)
- Heraeus Electronics (6-310)
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AI & Data Centers Stage

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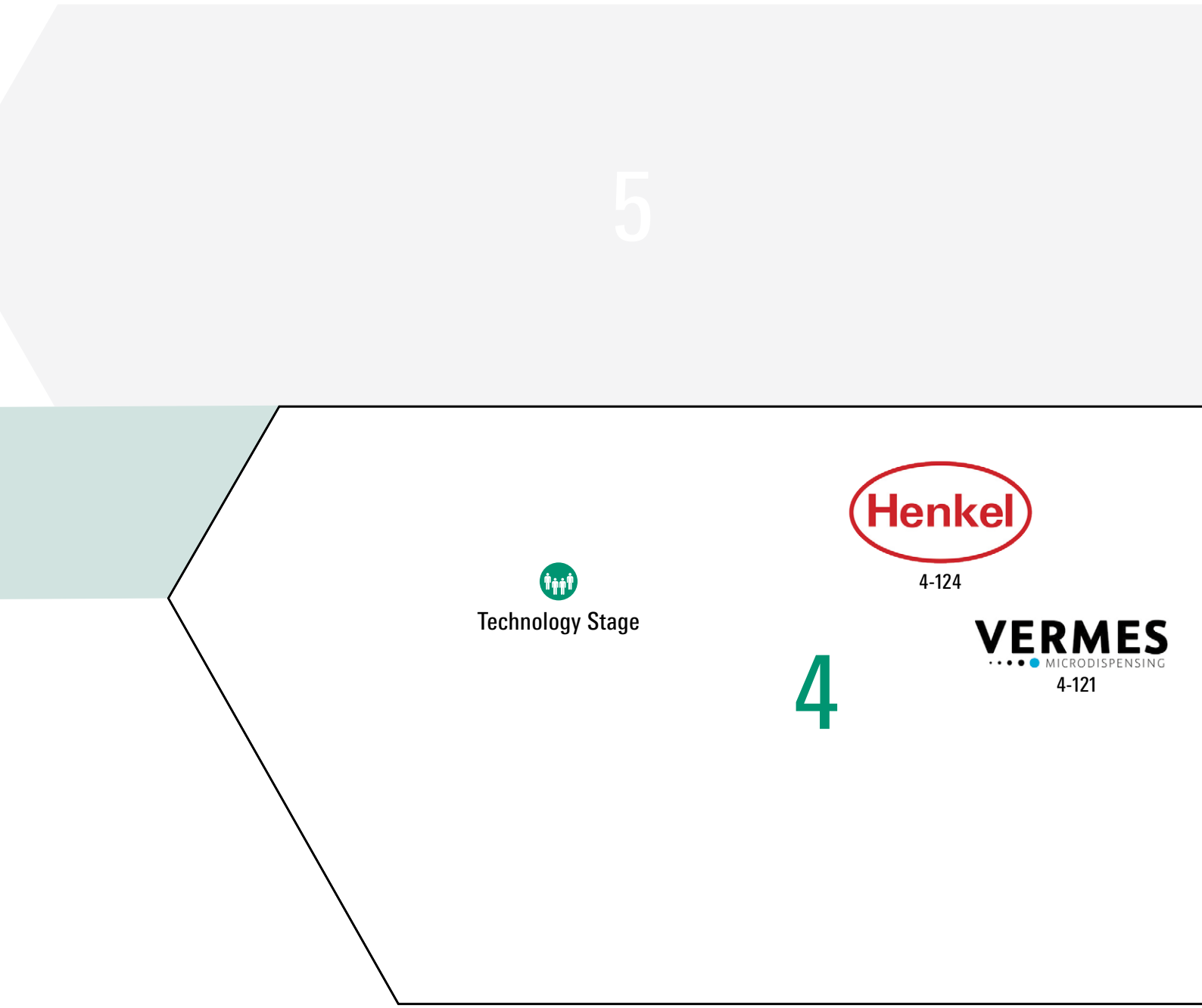

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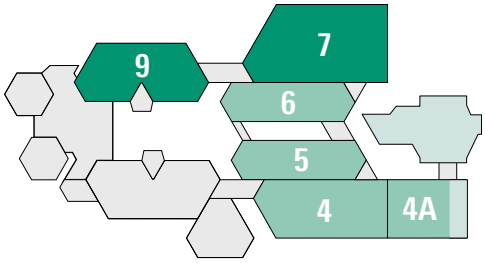

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TOSHIBA
4A-227

4A

Exhibitor Stage

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Poster Sessions

This company offers products for E-Mobility/Energy Storage

Hall 4A

- NOVOSENSE Microelectronics (4A-119)
- KERAFOL Keramische Folien (4A-110)

Ideas in Motion: Empowering the Future of Electrification and Industrial Automation

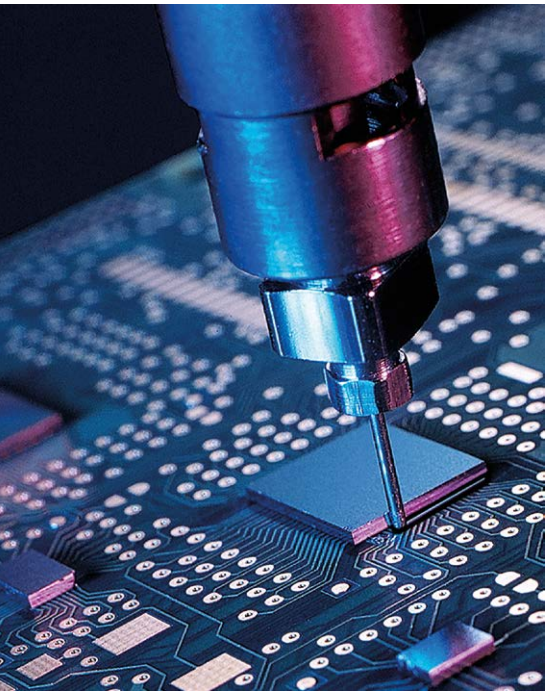
Nearly every aspect of modern life is affected by electronics in some way. From the vehicles we drive to the smart factories that manufacture our goods, people depend on technology for work, leisure, health, and comfort. Disruption, inconvenience, and even life-threatening conditions can result when electronics fail. In an era defined by rapid technological shifts, safeguarding these systems is not just an option—it is a foundational necessity for the future.

The Megatrends Shaping Our World

We are living in a transformative period where two massive megatrends are reshaping the global industrial and consumer landscapes: Industrial Automation and Electrification. The transition towards sustainable energy and interconnected smart manufacturing is accelerating at an unprecedented pace. At Henkel, we capture this momentum under our campaign of Ideas in Motion. This concept enables our partners to scale by empowering them with advanced material science solutions.

The Electrification Imperative

The push towards comprehensive electrification—spanning electric mobility (e-mobility), renewable energy generation, and advanced power grids—is fundamentally altering how we generate, distribute, and consume power. Electric vehicles are demanding higher range and faster charging times, which in turn requires power electronics that can handle massive voltage and current loads without degrading. Similarly, the infrastructure supporting this shift, from solar inverters to high-voltage grid stations, must operate flawlessly for decades under constant stress. Electrification is no longer a niche market; it is the baseline for future global infrastructure.



The Rise of Industrial Automation

Simultaneously, industrial automation is driving the fourth industrial revolution (Industry 4.0). Modern factories are becoming increasingly autonomous ecosystems. They rely heavily on interconnected Internet of Things (IoT) devices, sophisticated sensors, edge computing, and robotics that must operate with absolute precision around the clock. In these environments, tolerance for downtime is practically zero. A single failure in a sensor or a motor control unit can bring an entire production line to a halt, resulting in catastrophic financial losses and supply chain disruptions.

As we demand higher performance and seamless connectivity, the underlying electronic systems are being pushed to their absolute limits in increasingly harsh environments." However, these megatrends bring profound engineering challenges. The electronic systems driving these megatrends are deployed in increasingly brutal environments, subjected to extreme temperatures, mechanical vibration, moisture, and chemical exposure. When high-performing, dependable electronics are non-negotiable, the focus must shift to how we protect these vital investments from the inside out.

The Core Challenge – Managing Complexity, Heat, and Harsh Environments

As electronic systems integrate more capability into increasingly challenging, complex designs and highly compact footprints, their inherent vulnerability increases. The miniaturization of components means that power densities are rising at a staggering rate. While smaller, more powerful devices are the goal, they bring a silent but highly destructive by-product: Heat.

The Critical Role of Thermal Management

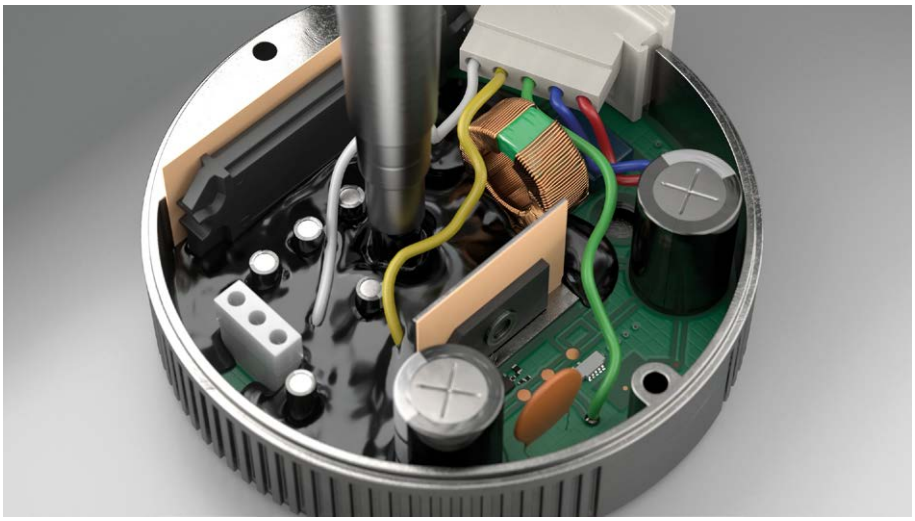
Efficient heat control is no longer a secondary consideration; it is an absolute necessity for system viability and safety. If potentially damaging heat is not rapidly and effectively dissipated across electronics applications, the performance degrades exponentially, and the operational lifetime of the device plummets. In high-power applications like EV battery management systems or industrial motor drives, excessive heating can lead to thermal runaway, causing complete system failure or even fire hazards. Traditional cooling methods often fall short in modern, tightly packed architectures, necessitating advanced thermal interface materials that can bridge the gap between heat-generating components and heat sinks at a microscopic level.

Defending Against the Elements

Beyond thermal management, the physical safeguarding of function is vital. Protection materials are some of the most critical elements of next-generation electronic system design. The modern printed circuit board (PCB) or power module might be a marvel of electrical engineering, but without the right encapsulation, coating, or underfill, it remains entirely exposed to real-world operational hazards.

Moisture can cause short circuits and corrosion; dust and metallic particles can bridge connections; and constant vibration in automotive or industrial settings can physically break solder joints. Defending electronics against these various contaminants and environmental exposure extremes is the only way to secure operational reliability and prolong useful lifetime.

This requires a holistic approach to material selection—one that views protective and thermal materials not as an afterthought applied at the end of the line, but as an integral structural component of the electronic system from the very first design phase.



Proven Protection – Henkel's Solutions for Next-Generation Designs

To address these escalating industry demands, Henkel has developed a high-performance materials portfolio specifically engineered for the rigors of modern power electronics. We understand that safeguarding function and extending the useful life of electronic systems are vital to protecting your investment.

Award-Winning Thermal Solutions

Henkel's innovative thermal management solutions portfolio is designed to address and dissipate potentially damaging heat across a vast array of electronics applications. Utilizing multi-award-winning formulations in various mediums—including phase change materials, thermal greases, gap pads, and liquid gap fillers—Henkel provides tailored thermal management materials that help in enabling optimal performance and significantly extending device lifetime.

Comprehensive Protection Portfolio

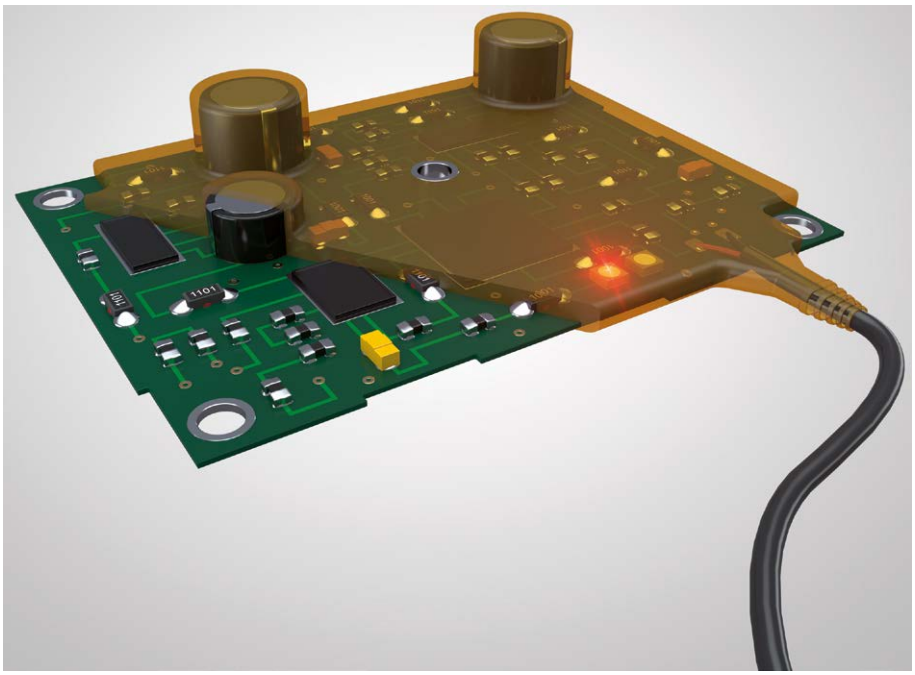
Our protection portfolio goes beyond heat management to offer an impenetrable shield against mechanical and environmental stress. This includes board-level underfills that reinforce brittle solder joints against thermal cycling and shock, ensuring the physical integrity of the board.

At this year's exhibition, Henkel's booth will feature a curated display of our key portfolio, highlighting recent, groundbreaking innovations for industrial electronics. We invite you to explore our advanced solutions:

- **Advanced Potting Solutions:** We are highlighting high-reliability encapsulants such as LOCTITE STYCAST US 8000. Designed for rugged environments, this potting material offers superior protection for sensitive components against moisture, chemicals, and mechanical shock, ensuring long-term stability in power applications.
- **Low-Pressure Molding Materials:** Discover the efficiency of the three-step low-pressure molding process with TECHNOMELT PA 6370. This innovative material encapsulates, seals, and protects in a fraction of the time required by traditional potting, offering a lightweight, environmentally responsible solution that streamlines manufacturing.
- **Conformal Coating Solutions:** Explore the robust environmental defense provided by LOCTITE STYCAST CC 8555. This advanced coating conforms seamlessly to the PCB topography, providing a critical barrier against humidity, dust, and harsh industrial atmospheres without adding significant weight or volume.

Experience the Innovations Live

Each product design is unique, and the material requirements are highly dependent on your specific operational needs and manufacturing processes. The dedicated product wall at our booth will showcase our extensive range of thermal management and protection products. Furthermore, visitors can experience the precision of our solutions firsthand during a live underfill application demonstration directly at the booth. Let's put your Ideas in Motion. Visit the Henkel experts in Hall 4, Stand 4-124 to discuss your specific engineering challenges and gain the expert material solutions needed to secure your next-generation designs.



Vertiv Partners with Yokogawa for AI-ready UPS Systems Validation

Artificial Intelligence has fundamentally altered power dynamics within data centers. Unlike traditional workloads with slow and predictable power variations, modern AI creates “pulsed loads”, where processors switch rapidly between idle and full capacity. Power demand can swing from 0% to 100% and back in milliseconds, creating erratic “on-off” cycles that place power infrastructure under severe stress.

Uninterruptible power supply (UPS) systems must now also function as a dynamic power conditioner capable of reacting to these variable load swings in real time. If it cannot manage these pulses effectively, they can be reflected back to the grid or backup generators, threatening overall system stability or even breakdown.

Vertiv provides critical infrastructure technologies, including large power converters. Its Power Center in Bologna needed to validate new Input Power Smoothing algorithms for its Vertiv™ Trinergy™ UPS systems. These intelligently draw energy from the UPS batteries during peak pulses, shielding the upstream generator from the erratic behavior of an AI load.

The units have a sophisticated topology, featuring two AC three-phase mains and one DC battery input, and one three-phase output. Each required monitoring simultaneously. Teams needed to capture long-duration thermal data and high-speed resolutions to analyze waveform deformation, noise, and Total Harmonic Distortion (THD) during rapid switching events. Active, reactive, and apparent power also had to be characterized to fully understand power quality under stress.

With high channel counts, currents of up to 5000 A demanding strict safety controls, and a need for 24/7 reliability, intermittent anomaly capture, and long-term thermal stability logging, the instrumentation challenge was considerable.

Veritiv created a fully integrated measurement ecosystem from Yokogawa, anchored by the WT5000 Precision Power Analyzer, DL950 ScopeCorder, GM10 Data Acquisition System, and tied together by the IS8000 software platform.

The WT5000 Precision Power Analyzer provides primary power analysis. With a power accuracy class of 0.03% and support for up to 7 input modules, it allows Vertiv engineers to measure AC and DC power simultaneously. The instrument provides harmonic analysis up to the 500th order, essential for evaluating power quality and validating efficiency even under dynamic load conditions.

The DL950 ScopeCorder captures the transient behavior of the “pulsed loads”. Configured with 16 channels, it combines the benefits of a high-speed oscilloscope with a long-term data recorder. It captures the specific shape of voltage and current waveforms during rapid switching events, allowing engineers to identify high-frequency noise and verify the system’s dynamic response time without missing critical details.

Connecting these domains is Yokogawa’s IS8000 software, which synchronizes the instruments using the IEEE 1588 Precision Time Protocol (PTP). This platform integrates data from the WT5000, the DL950, and the GM10, which monitors thermal points across the system. This setup creates a single, time-aligned dataset where thermal stress, power efficiency, and waveform distortion can be viewed side-by-side.

Luigi Balma of the Vertiv R&D team explained, “The Yokogawa ecosystem is the best solution for us because it allows us to see so many different variables - voltage, currents, DC and AC - at the same time on a single display, and coherent in time.”

As well as directly enabling the validation of their patented Input Power Smoothing technology, the integrated solution has transformed the Bologna laboratory’s workflow. Being able to view thermal, electrical, and waveform data on a single IS8000 interface has significantly reduced testing complexity and debugging time. Using Yokogawa’s precision validation, Vertiv continues to develop next-generation data center technology.

Breaking the Control Bottleneck: Democratizing FPGA Technology in Power Electronics

As wide-bandgap semiconductors and complex inverter topologies push traditional microcontrollers to their limits, Field Programmable Gate Arrays (FPGAs) offer a powerful, flexible alternative. With its new FPGA-Rapid-Prototyping-System (FRPS), Tetranes is now removing the steep learning curve, enabling engineers to harness true parallel processing for next-generation power electronics. The power electronics sector is undergoing a massive transformation, driven largely by the demands of e-mobility and renewable energy integration. Today's systems rely on highly complex, dynamic algorithms to maximize efficiency. A prime example is the shift towards multi-level, fast-switching inverters, which significantly reduce harmonic distortion and minimize the need for bulky passive components. Furthermore, the implementation of advanced control strategies, such as Model Predictive Control (MPC), requires immense computational power. MPC evaluates the effects of all possible switching states in real-time over multiple predictive steps—a task that pushes conventional control hardware to its breaking point.

The Limits of Traditional Microcontrollers

This computational demand is exacerbated by the rise of Wide-Bandgap (WBG) semiconductors like Silicon Carbide (SiC) and Gallium Nitride (GaN). These materials allow for much higher switching frequencies, demanding lightning-fast signal processing. While modern microcontrollers feature integrated hardware cores for Pulse Width Modulation (PWM) or Space Vector Modulation (SVM), they are inherently limited by their sequential processing architecture and hardwired peripherals. For R&D departments looking to innovate beyond standard, fixed modulation schemes, these rigid microcontroller structures often become a developmental bottleneck.

The FPGA Advantage and the "Skill Gap"

Field Programmable Gate Arrays (FPGAs) present the ideal solution. Unlike sequential microcontrollers, FPGAs allow engineers to create customized hardware and software architectures on a single chip. Because multiple process structures can be implemented simultaneously, control algorithms are executed in true parallel, offering unmatched performance and flexibility. However, there is a reason FPGAs are not yet the ubiquitous standard in power electronics: The barrier to entry is notoriously high. Developing for FPGAs traditionally requires specialized expertise in Hardware Description Languages (HDL)—a skill set deeply rooted in telecommunications and signal processing, but relatively rare among power electronics engineers.

Tetranes FRPS: Bridging the Gap

To overcome this exact challenge, Tetranes has developed the FPGA-Rapid-Prototyping-System (FRPS). This modular, FPGA-based development environment is specifically designed to make high-end processing accessible to power electronics developers without requiring them to become HDL programming experts. The FRPS is built around a rack-mounted modular architecture. At its core is a central FPGA processing card, which can be seamlessly customized with various expansion modules for specific tasks, such as high-speed inverter communication or analog data acquisition. The greatest advantage of the FRPS is its ability to decouple software innovation from hardware limitations. Engineers can design, simulate, and implement custom multi-level control systems (3-level or N-level) directly on the platform without constantly redesigning the underlying printed circuit boards. It even opens the door to experimenting with entirely new, non-PWM modulation techniques. Ultimately, the Tetranes FRPS provides R&D teams with a highly flexible, modular sandbox.

Competence in Power: Ainuo and HEIDEN Join Forces

As the demand for energy-efficient power electronics testing grows, Ainuo Instrument Co., Ltd. and German-based HEIDEN power GmbH have entered a strategic partnership. The result is the cutting-edge ANRGL(F) Series Regenerative Grid Load, designed to set new standards in four-quadrant operation and energy recovery. The transition towards renewable energy and e-mobility requires testing equipment that is both highly precise and exceptionally efficient. Addressing this industry demand, Ainuo and HEIDEN power have united under the motto "COMPETENCE IN POWER." This collaboration leverages Ainuo's advanced digital control methods and HEIDEN power's established European market expertise, delivering robust solutions for complex power testing environments.

Technological Innovations

At the core of this partnership is the ANRGL(F) Series Regenerative Grid Load. Engineered with advanced SPWM technology and FPGA digital processing, this system offers versatile AC, DC, and AC+DC output modes. A key differentiator in today's energy-conscious market is its ability to operate as a constant current source across all four quadrants with 100% rated power feedback to the grid. By returning power efficiently to the grid instead of dissipating it as heat, the system significantly reduces energy waste and lowers operational costs—a crucial advantage for facilities running large-current test conditions.

Advanced Testing Capabilities

To meet rigorous design and production verification requirements, the ANRGL(F) series features comprehensive harmonic synthesis, capable of generating 2 to 50 times interharmonics with a synthesis bandwidth of 3,000 Hz. The system scales effortlessly, reaching up to 180 kVA capacity through single-phase or three-phase parallel operation.

Combined with an intuitive 8-inch color LCD and fully programmable sequence modes, the equipment is perfectly suited for device manufacturers, quality inspection centers, and certification bodies testing low voltage distribution devices. Ultimately, the Ainuo and HEIDEN power partnership provides the power electronics industry with a highly adaptable, energy-efficient testing solution for the future.

Power GaN market accelerates amid strategic shifts and new entrants

Ecosystem transformation, datacenter momentum, and technology diversification reshape the competitive landscape.

By Roy Dagher, Technology & Market Analyst, Compound Semiconductors at Yole Group

The power GaN market is entering a new phase of acceleration, driven by evolving market dynamics, strategic repositioning among key players, and expanding application opportunities. In 2025, the rise of AI-driven datacenters fueled market growth. At the same time, the ecosystem is undergoing structural changes marked by mergers and acquisitions, new partnerships, and diversification in manufacturing strategies. These developments, deeply analyzed in Yole Group's Power SiC/GaN Compound Semiconductor Market Monitor - Q1 2026, are redefining competitive positioning and setting the stage for the next wave of adoption.

Datacenter Pull and Industry Reshaping: A Market in Acceleration

The market is expected to see significant growth in the coming quarters. A key driver of this expansion is the growing adoption of GaN technologies in datacenter applications, where efficiency and power density are critical.

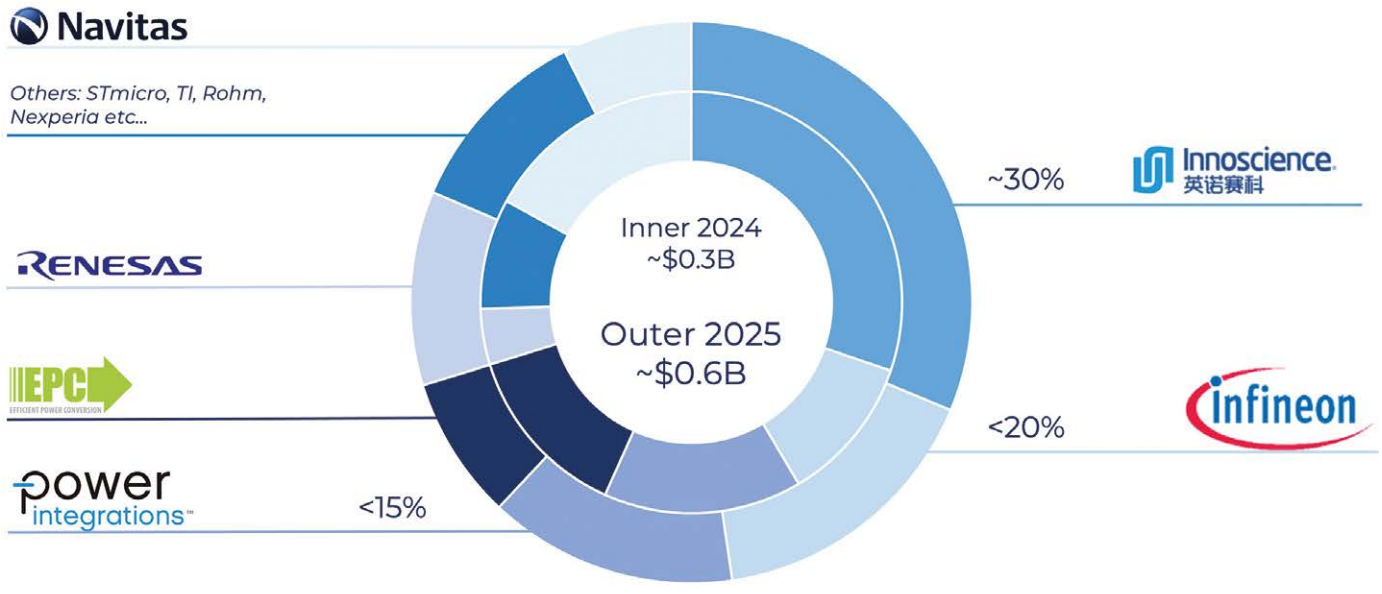
Recent years have also been characterized by strong consolidation.Major acquisitions, such as Infineon Technologies' 830 million dollar purchase of GaN Systems and Renesas' 339 million dollar acquisition of Transphorm, highlight the strategic importance of GaN. In parallel, Innoscience's IPO signals growing investor confidence in the technology. These moves raise questions about the potential for further acquisitions and large-scale investments as competition intensifies.

The competitive landscape is evolving rapidly. Innoscience remains the market leader in 2025, leveraging its expansion into automotive, datacenter, and home appliance applications, as well as humanoid robots. Its strategy of broadening its portfolio through power modules and Epiwafers reinforces its market reach. Infineon Technologies has significantly increased its market share, supported by strong momentum in datacenters, renewable energy, and consumer segments. Renesas is also strengthening its position through a diversified product offering across multiple applications.

Meanwhile, Navitas is undergoing a strategic shift, moving away from lower-margin fast-charging markets toward higher-value, higher-power applications. This new market positioning has led to a temporary loss of market share but reflects a long-term value-driven strategy.

onsemi's Strategic Entry: Fast-Track Adoption Meets Long-Term Differentiation

A notable development in 2025 is the entry of onsemi into the power GaN market. As one of the top three power device manufacturers,



*All detailed market shares are available in Yole Group's product

The growing role of datacenters, combined with increasing adoption across industrial and consumer segments, is creating strong momentum for the GaN technology (Image: Yole Group).

Roy Dagher, Yole Group: "Meanwhile, Navitas is undergoing a strategic shift, moving away from lower-margin fast-charging markets toward higher-value, higher-power applications. This new market positioning has led to a temporary loss of market share but reflects a long-term value-driven strategy."

onsemi previously focused on silicon-based technologies, including MOSFETs, IGBTs, and SiC. Its move into GaN marks a significant strategic shift.

In October 2025, onsemi introduced vertical GaN (vGaN) technology targeting 700 V and 1200 V power devices, aiming to build long-term differentiation in high-voltage applications. Shortly thereafter, the company announced partnerships with Innoscience and GlobalFoundries to address the 40 V to 650 V range using GaN-on-Si technology. This dual approach enables onsemi to accelerate time-to-market for mid-voltage applications while investing in future high-voltage innovation.

The company's sudden entry underscores the increasing importance of GaN in the power electronics landscape. Initial GaN samples are expected in the first half of 2026, with revenue generation anticipated by 2027. This timeline reflects both the maturity of the technology and the competitive urgency among leading players. The power GaN market is undergoing a profound transformation, driven by shifting market dynamics, expanding applications, and intensified competition. The growing role of datacenters, combined with increasing adoption across industrial and consumer segments, is creating strong momentum for the technology. At the same time, strategic moves, from acquisitions to new market entries, are reshaping the competitive landscape.

As more players invest in GaN and diversify their approaches, the ecosystem is becoming more complex and dynamic. The coming years will likely see continued consolidation, innovation in manufacturing and packaging, and accelerated adoption across high-growth applications.

In this evolving environment, the ability to combine technology differentiation with strategic positioning will be key to capturing value in the next phase of the power GaN market. eg

Image: death_rip/stock.adobe.com

PCIM Top Innovation

The inaugural PCIM Top Innovation shines a spotlight on groundbreaking innovations in power electronics. Wolfspeed won the first award for its 10 kV SiC MOSFET. If you want further information about the PCIM Top Innovation Award come to Stand 5-130 in Hall 5.

Wolfspeed's device has a breakdown voltage of 10 kV and an on-resistance of 305 mΩ at a rated current of 20 A, and due to their unipolar operation, SiC MOSFETs enable significantly lower switching losses and higher switching speeds than IGBTs. They also possess an intrinsic parasitic body diode that can be utilised in reverse current operation. A well-known reliability issue with high-voltage-resistant SiC devices is bipolar degradation (BD). When current flows through the body diode, minority charge carriers are injected, causing existing crystal defects, particularly basal plane dislocations, to expand irreversibly. This increases the forward voltage of the diode and can compromise the device's reliability. According to the manufacturer, a key technical feature of the presented MOSFET is its ability to control or prevent these degradation mechanisms, even when the body diode is in use. Wolfspeed's TDDB (time-dependent dielectric breakdown) analyses indicate a theoretical lifetime of up to 158,000 years at a continuous gate bias voltage of 20 V.

Realizing Pulsed-Power Potential: Enabling Next-Generation Applications

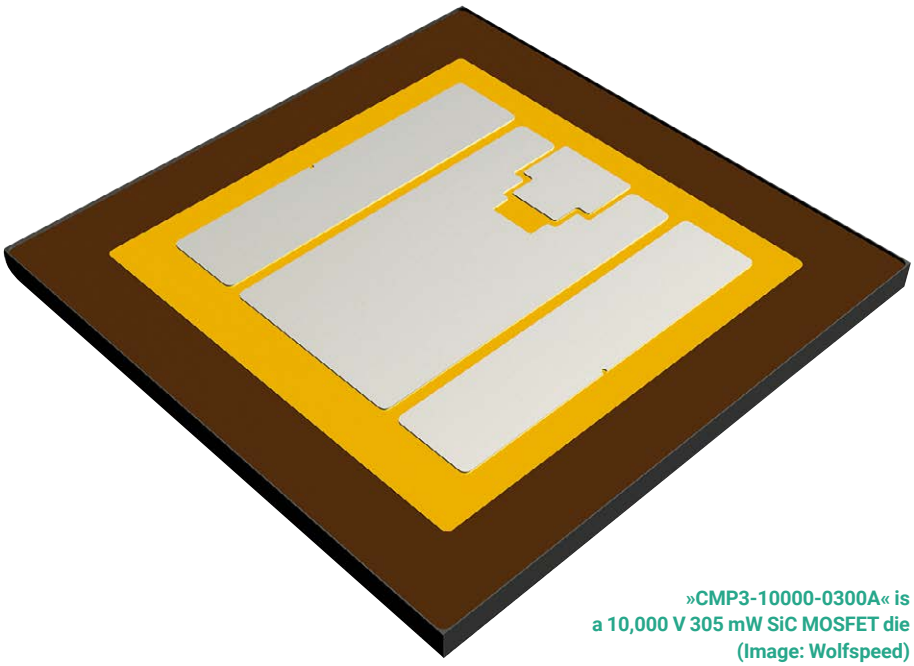
With a rise time of less than 10 nanoseconds, the new technology can replace conventional mechanical spark-gap switches, which degrade over time due to high-current, high-temperature arcing. This increases maintenance costs and the total cost of ownership. The new technology uses SiC MOSFET-based solid-state switches. These solid-state devices eliminate arcing and enable efficient energy transfer and improved timing precision for pulsed power transfer. They also reduce size and system complexity for high-performance pulsed-power applications, including geothermal power generation, power generation for AI data centers, semiconductor plasma etching and sustainable fertiliser production.

Powering AI with reliable silicon carbide-based solid-state transformers

Ashish Kumar, Ph.D., MHV Research Scientist at Wolfspeed, describes an application for which the new silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) are particularly well suited: AI Data centers. He mentions a major infrastructure challenge in the expansion of AI Data centers: the short supply of conventional medium-voltage transformers, with

lead times of up to three years. Solid-state transformers (SSTs) are being discussed as an alternative. These power electronic systems can convert medium-voltage AC directly into the DC required by Data centers. Compared to traditional iron-core transformers, SSTs offer faster controllability, potentially more compact designs, and a modular architecture.

The grid connection for Data centers typically ranges from 13.8 to 35 kV AC. SSTs comprise several power electronic converter cells for this purpose. Multi-level architectures with devices connected in series are usually required when using SiC devices with breakdown voltages below 5 kV. Conversely, high-voltage-capable SiC devices above 5 kV enable simpler topologies with fewer cells.



»CMP3-10000-0300A« is a 10,000 V 305 mW SiC MOSFET die (Image: Wolfspeed)

According to Wolfspeed, their 10 kV SiC MOSFET CPM3-10000-0300A is a key component for such high-voltage SSTs. For compact SSTs, switching frequencies above 10 kHz are important as they reduce the size and weight of magnetic components. However, high-voltage silicon IGBTs with typical reverse voltages of around 6.5 kV are usually only suitable for switching frequencies in the range of a few hundred hertz due to high switching losses.

High switching frequencies are crucial for SST applications because the required magnetic components, particularly coils and transformers, can be designed to be much smaller and lighter at higher frequencies. Typical target values are above 10 kHz. However, conventional high-voltage silicon IGBTs with reverse voltages in the range of 6.5 kV are generally only suitable for a few hundred hertz due to high switching losses, meaning they are not ideal for compact SST designs. SiC MOSFETs enable significantly lower switching losses and faster switching operations due to their unipolar structure.

Features

- Easy to parallel and simple to drive
- Temperature-independent high-speed switching
- Enhanced Reliability
- Maintains reliable performance during reverse power flow

Typical Applications

- Pulsed Power
- Medium-Voltage Drives
- Solid-State Transformers
- Smart Grid/Grid-Tie Distributed Generation
- Medium-Voltage UPS Systems
- Nuclear Power Generation for AI Data Centers

Features and areas of application summarized (Image: Wolfspeed)

Absolute Maximum Ratings

Stress beyond those listed under absolute maximum ratings may damage the device.

Parameter	Symbol		Rating	Unit
Drain-Source Voltage, across T_{VJ}	$V_{DS(max)}$		10000	V
Maximum Gate-Source Voltage, Peak Transient Capability	$V_{GS(max)}$		-10/+25	V
Static Gate-Source Voltage	$V_{GS(op)}$		-5/+20	V
Continuous Drain Current[1]	I_{DS}	T_c = 25 °C	20	A
		T_c = 90 °C	15	
Pulsed Drain Current, t_p limited by $T_{VJ(max)}$	$I_{DS(pulse)}$		40	A
Virtual Junction and Storage Temperature	T_{VJ}, T_{stg}		-55 to +175	°C
Maximum Processing Temperature, in non-reactive ambient	T_{proc}		325	°C

Note 1. Assume testing at V_{GS} = +20 V, with a junction-to-case thermal resistance $R_{TH(J-C)}$ = 0.34 °C/W.

Absolute Maximum Ratings (Image: Wolfspeed)

Kumar once again refers to the reliability issue caused by the bipolar degradation of the intrinsic body diode and elaborates: 'In our 10 kV SiC MOSFET, no bipolar degradation occurred during Body Diode Operating Life (BDOL) tests lasting over 1,000 hours.'

Sensitivity to cosmic radiation is another important reliability requirement in high-voltage operation, as high-energy particles can trigger single-event failures, particularly at high reverse voltages. According to Kumar, the device exceeds industry-standard requirements for the failure-in-time (FIT) rate by a factor of four during typical operation at 6,000 V DC.

Summary of the benefits

- Reduce system cost by approximately 30%: Using 10 kV SiC allows designers to consolidate multi-cell designs into fewer cells and downsize three-level inverters to a two-level topology
- Improve power density by more than 300%: Increasing switching frequencies from 600 Hz to 10,000 Hz simplifies control and gate drive circuitry, while also shrinking magnetics
- Reduce system-level thermal requirements by up to 50 %: Achieving 99 % conversion efficiency enables better thermals than IGBTs.
- Wolfspeed was awarded with the first PCIM Top Innovation – let's see who wins it next year! As an exhibitor of the PCIM you are welcome to simply submit innovative developments when the next call for entries is announced. st

The Silent Switches of Electrification: From Thyristors to WBG

Over the last five decades, technological advances in power semiconductor devices have driven the development of power electronic converters and their system integration, making these devices the key technology for power electronics as a whole. This includes power supplies ranging from milliwatts to megawatts, inverters, motor control and traction converters for all transport vehicles, whether on the road, rail, in the air or on water, as well as their charging infrastructure.

By Prof. Leo Lorenz, President of the European Centre for Power Electronics (ECPE)

The performance of power electronic systems has always been, and continues to be, directly linked to the characteristics of the available semiconductor technologies. In this sense, power semiconductors have been the driving force behind electrification for decades.

The bipolar era: The Dawn of Modern Power Electronics

The history of power semiconductors dates back to the mid-1950s. The first qualified power diodes came onto the market at this time, enabling more compact and efficient rectifiers than the electromechanical or valve-based solutions that had been available until then. However, the real breakthrough followed shortly afterwards with the introduction of the thyristor by General Electric in 1956 and by Siemens in 1957. This made it possible to control the switching of high electrical power using a semiconductor device for the first time.

The thyristor was a revolutionary development for its time. It could block high voltages and switch large currents, opening up entirely new possibilities in industrial power conversion. In the decades that followed, this technology developed rapidly. Starting with the first devices in the early 1960s, which had voltage ratings of 1.5 kV and 100 A, increasingly powerful switches were developed for large-scale industrial applications, traction systems, and power transmission using light-triggered thyristors with ratings of up to 8 kV and 6 kA. These components remain crucial to high-power applications in power transmission and industrial processes in the high megawatt range to this day.

Physically, the thyristor is based on a bipolar charge carrier distribution, also known as an electron/hole plasma. Its excellent conduction properties are due to conductivity modulation: the injection of electrons and holes significantly increases the conductivity of the semiconductor structure, enabling low conduction losses. This property has made the thyristor the component of choice for high-power applications for decades.

However, the classic thyristor had one crucial limitation: while it could be switched on actively, it could not be switched off actively. Once triggered, it remained conductive until the current fell below a certain holding cur-

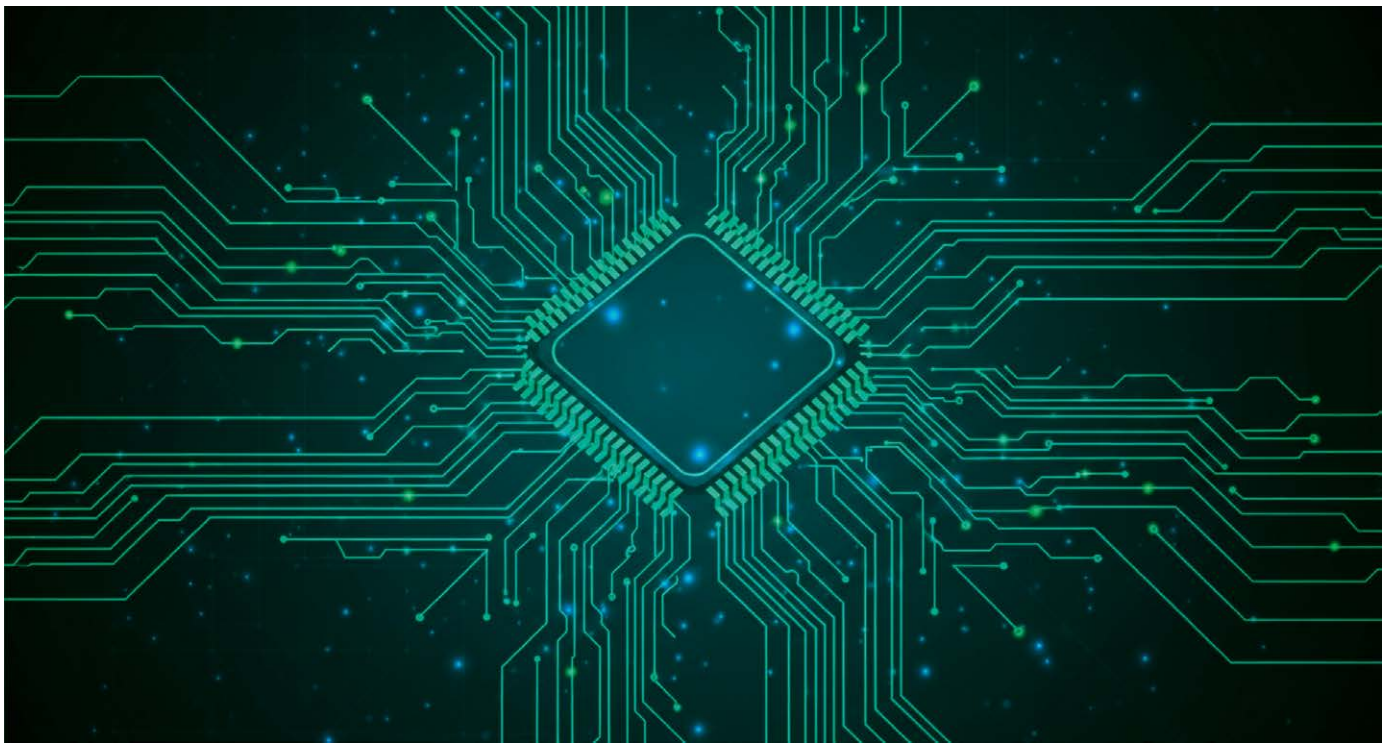


Image: yari/stock.adobe.com

rent, either at the natural zero-crossing point in AC operation or with the aid of external commutation circuits. This made system architecture complex.

A significant development was therefore the Gate Turn-Off Thyristor (GTO), which became important in industry in the late 1960s and 1970s. For the first time, it enabled this thyristor structure to be switched off actively via the gate. However, this progress came at a high cost. In the case of large devices, switching off requires very high gate currents, placing high demands on the design of the driver circuits and requiring considerable expertise. Furthermore, there was a fundamental physical conflict: a device whose conductivity is strongly modulated offers excellent conduction properties, but it also stores high charges that must be discharged during switching off. With the GTO, therefore, a compromise had to be found between good conduction losses and controllable turn-off.

Meanwhile, bipolar power transistors (BJTs) became increasingly important in the 1960s and 1970s. Unlike thyristors, BJTs could be switched on and off actively at any time, just like GTOs. This significantly simplified the implementation of many power electronics circuits, as the complex commutation networks mentioned earlier were no longer necessary. The key advantage of BJTs over GTOs was their significantly simpler and faster controllability at low to medium power levels. Furthermore, switching frequencies in the kilohertz range were possible, which was a considerable advance on earlier designs.

However, bipolar power transistors also had their limitations. While they were easier to drive than GTOs, the process was still relatively complex due to the requirement for a continuous base current. Even more problematic was their limited safe operating area (SOA). The so-called 'second breakdown' in particular posed a serious problem, as local thermal instabilities could lead to the device failing suddenly, even if the nominal limit values appeared not to have been exceeded at first glance. In practice, this meant that bipolar power transistors could only be operated within a restricted SOA range.

A crucial and deep going technology cut came with the MOS revolution

The transition to MOS-controlled power semiconductors in the late 1970s was a significant technological development. A key milestone was reached in 1979 when International Rectifier introduced one of the first commercially successful power MOSFETs. This ushered in the era of modern MOS-controlled power electronics.

Initially, this development took place within the low-voltage range. The first power MOSFETs were designed for 50 V and 100 V voltage ranges – unremarkable by today's standards, but highly significant from a technological perspective at the time. This is because these components combined the electrical, thermal, and drive characteristics that system developers had long sought.

Unlike a bipolar power transistor, a power MOSFET does not require continuous control current. The gate is electrically isolated, so only its input capacitance, which is determined by the cell structure, needs to be recharged to drive it. This significantly simplifies the driver circuit while enabling precise control of the switching edges and management of the protection functions. In addition, the power MOSFET operates as a unipolar device without minority charge storage, enabling high switching frequencies.

Another decisive advantage lies in its operational behavior. While the safe operating area (SOA) range of bipolar power transistors was severely limited by second-breakdown effects, that of a power MOSFET approaches a rectangular characteristic curve much more closely. This does not mean that MOSFETs can withstand unlimited stress, as thermal, electrical and robustness limits still apply, but they can be operated much closer to their specified operating limits than bipolar power transistors.

The fact that this technology was quickly recognized as groundbreaking is evident from the subsequent entry of other major manufacturers, including Siemens, into the market with their own power MOSFETs.

However, the transition to MOS technologies meant more than just a new component; it also represented a fundamental shift in manufacturing. While many bipolar power semiconductors could still be manufactured using traditional discrete processes, power MOSFETs required IC-compatible technologies, necessitating high investment. This resulted in a significant shift in the market in favor of financially robust manufacturers, as smaller companies could not afford the necessary production facilities.

The development of the power MOSFET represented a revolutionary step not only in manufacturing technology, but also in the development of power electronic energy converters. With the power MOSFET, switch-mode power supplies (SMPS) could now be manufactured with high power density, i.e. small size and weight, while maintaining high efficiency. This opened up a high-volume field of application for power supplies in the consumer sector, ICT (information and communications technology), and data processing. The next step, starting around the 1990s, was the integration of the drive and protection circuitry – the so-called SMART FET – which led to the electrification of automobiles. Many previously mechanical switches, such as relays and fuses, were replaced by SMART FETs. With increasing system integration, this led to significant energy savings, higher reliability and a smaller footprint.

However, this technology has also reached its physical limits. The classic silicon MOSFET is a unipolar device. Unlike bipolar switches, it cannot modulate its conductance when switched on. As the reverse voltage increases, the drift region must be made thicker and less heavily doped, significantly increasing the on state-resistance. Consequently, the economically viable operating range for traditional silicon power MOSFETs has historically been limited to a few hundred volts.

The path to higher voltages: BiMOS, IGBT and super-junction

Following the initial success of low-voltage power MOSFETs, the appeal of MOS-controlled operation became apparent. The obvious question, therefore, was how these advantages could be extended to higher voltage ranges.

One early interim solution was the BiMOS concept, which combined MOS and bipolar transistor technologies. The aim was to combine the simple, voltage-controlled operation of MOS technology with the high-voltage capability of bipolar power semiconductors. While these concepts were important intermediate technological steps, they were superseded by the IGBT (Insulated Gate Bipolar Transistor), which possessed precisely these characteristics: a MOS control gate, a long drift region for voltage build-up and a back-doped p-region for hole injection.

Its breakthrough came in the mid-1980s. The IGBT combines the simple gate control of a MOSFET with the excellent conductivity of bipolar power semiconductors. Physically, it utilizes conductivity modulation in the drift region through electron and hole injection, achieving significantly lower conduction losses at high voltages than a purely unipolar MOSFET.

Consequently, the IGBT has become a vital component in many modern power electronic converters across various industrial, mobility and energy supply applications. The IGBT has revolutionized the entire field of electric drive technology with variable speed control, including industrial electric drives and high-power converters extending into the multi-megawatt range for use in process technology, renewable energy generation and power transmission. Without this component, traction converters in e-mobility on road, rail or water would be almost inconceivable in their current form. Electric motors account for more than 50 per cent of global electricity consumption, and it is precisely here that the IGBT has made energy-efficient, precisely controllable drive technology economically viable on a large scale. Reduced manufacturing costs, significantly increased power density for chips and power modules, and excellent robustness and reliability have enabled the successful implementation of electric drives ranging from low power – for example, domestic appliances such as fridges and washing machines – to several megawatts in the high-power range.

Meanwhile, the MOSFET continued to evolve. A major technological breakthrough was the introduction of the super-junction MOSFET. Unlike conventional silicon MOSFETs, the drift region of super-junction MOSFETs is based on a structure of alternating p- and n-doped columns. The space charges of these columns compensate each other out during reverse-bias operation. This enables the drift region to be heavily doped without affecting the breakdown voltage. This greatly reduces the turn-on resistance and, to some extent, overcomes the classic physical limitations of conventional silicon MOSFETs. Consequently, silicon MOSFETs have been able to penetrate 600 V, 650 V and 800 V voltage ranges cost-effectively. Although the area-specific on-resistance increases with rising reverse voltage, it does so much more slowly than in conventional structures. Through consistent technological advancements, the area-specific on-resistance has decreased by over tenfold in the last two decades while maintaining the same reverse voltage.

It's not just the cell structure that matters

Unlike in digital semiconductors, where technological development is primarily driven by 'feature size', power semiconductor devices are significantly influenced by the cell structure and drift region, which determine the quality of the material.

The drift region, which is responsible for the breakdown voltage, is a vital part of the active semiconductor material. Its thickness, doping and material quality are key determinants of the switch's performance. Therefore, expertise in power semiconductor development is not only required for the layout of the semiconductor cell or process miniaturization, but also for materials science, defect control, and mastery of vertical structures.

This also explains why power semiconductors have historically been outsourced to traditional foundries far less frequently than digital components. Mastering the material and vertical structure enables significant control over performance.

The wide-bandgap era: SiC and GaN

The development of wide-bandgap materials, particularly silicon carbide (SiC) and gallium nitride (GaN), has marked a significant milestone in power electronics converter and system technology. These extremely fast-switching components, which have low dynamic and static losses, open up new possibilities in the development of power electronic converters in terms of power density, efficiency, and dynamic system behavior whilst maintaining high robustness. Compared to silicon-based semiconductors, both materials offer physical advantages in terms of a higher breakdown field strength, greater temperature resistance and better switching characteristics as unipolar switches.

SiC is particularly well-suited to high voltages and power levels. It allows for one magnitude thinner drift zones together with two magnitude higher doping while maintaining the same breakdown strength, resulting in significantly lower dynamic and on state losses. SiC is therefore ideal for applications requiring high efficiency, high voltages or high switching frequencies. These include traction converters in electric vehicles, which following the mission profile typically experience partial-load and dynamic operating conditions, as well as high-power DC/DC converters, fast-charging infrastructure, industrial power converters, and highly efficient power supplies.

GaN truly shines at very high switching frequencies extending into the MHz range, while simultaneously delivering high power densities at the chip and system levels. Its excellent dynamic properties make it ideal for compact power supplies, Data centers, chargers, and increasingly, more demanding power electronics applications. GaN HEMT devices, which are commonly used today, are lateral transistors offering the major advantage of system integration. This enables control and protection functions, as well as complex system functions, to be implemented in a highly targeted, application-specific manner. A significant development is the MBGaN (monolithic bidirectional GaN) transistor. These transistors significantly simplify established power electronics topologies by reducing the required number of components and the associated control overhead, consequently reducing overall system complexity.

However, technological progress does not necessarily mean the rapid and complete replacement of silicon, despite what some experts may claim. In many segments, the transition is likely to be much slower than the shift from bipolar power semiconductor devices to MOS-controlled technologies. This is due to the excellent quality of Si wafer material, the enormous maturity of silicon manufacturing, low costs and ongoing challenges regarding material defects, yield, packaging and processing wide-bandgap materials.

In the field of GaN, there is also an intense debate about whether to use horizontal or vertical structures. Horizontal HEMT-based designs currently dominate due to their excellent switching characteristics and good integration potential. However, vertical structures could become relevant in the future for higher voltages. Nevertheless, they are significantly more technically challenging.

Is it better to have one large switching stage or many small ones?

As voltages rise, the focus shifts to mastering the overall system as well as the

individual component. Single switches capable of withstanding extremely high voltages — for example, in the range of 10, 15 or 20 kV — seem attractive at first glance. Fewer components, less complexity and a higher voltage withstand capacity would be achieved. In practice, however, the expertise lies in mastering the overall system. Today, many experts rely on multi-level topologies with several IGBTs (insulated-gate bipolar transistors) or other power semiconductors connected in series or cascaded when developing high-power applications. The advantage is that, instead of a single large voltage step, there are many smaller ones. This improves the current-voltage waveform, reduces dv/dt stress, minimizes electromagnetic compatibility (EMC) issues, and reduces the need for filtering.

While a single high-voltage switch may be technically feasible, it results in significantly larger voltage spikes, causing additional problems at the system level. Furthermore, many new requirements arise for packaging technologies. Therefore, the best component is not necessarily the best system solution.

In modern power electronics system engineering, packaging plays a key role

It is no longer just the semiconductor that determines the performance of a power converter. A significant proportion of the electrical and thermal performance, as well as the reliability and service life, is determined by the packaging — that is, the housing design, assembly and interconnection technologies, materials used for heat dissipation and matching the coefficients of thermal expansion, and the arrangement of the chips to minimize distributed capacitances and parasitic stray inductances. While the chip performs the actual switching function in conjunction with the module's internal parasitic components, the packaging must simultaneously meet several requirements, which are sometimes in conflict with each other:

- High electrical insulation
- Efficient heat dissipation
- Minimal parasitic inductance
- Low distributed parasitic capacitance
- High mechanical and electrical reliability and robustness
- Long service life

Packaging becomes a critical factor, particularly given the high switching speeds of modern silicon carbide (SiC) and gallium nitride (GaN) devices. Even the smallest parasitic inductances can cause significant overvoltages, high-frequency oscillations, and electromagnetic compatibility (EMC) problems at high current-change rates.

By Prof. Leo Lorenz, President of the European Centre for Power Electronics (ECPE)

At the same time, as power density increases, the challenge of thermal management also increases. Higher power dissipation within a smaller chip volume results in greater thermal stress and more stringent requirements for matching the thermal expansion coefficients of the materials used, as well as the interface technologies between the chip and heat sink and the cooling system itself. The development trend for all power semiconductors, including silicon and wide-bandgap technologies, is towards chip scaling, i.e. higher power densities. However, this also results in higher power dissipation densities. As power densities increase, the complexity of packaging technology and thermal management also rises.

New packaging concepts therefore rely on chip embedding, direct copper connections and sintering technologies instead of conventional solder joints, as well as high-performance ceramics that offer good thermal conductivity and high electrical insulation.

Higher voltages further intensify these requirements. In such cases, controlling the electric field distribution and ensuring creepage distances, as well as considering the partial discharge and insulation strength of the entire module, are paramount.

Another development involves highly integrated modules that bring power semiconductors, drivers, protection functions and, in some cases, sensor technology closer together.

Monolithically integrated bidirectional GaN switches also represent a promising development for the future. These will significantly simplify certain power electronics topologies, such as direct AC/AC converters and the cost-effective implementation of constant-current converters for motor control and matrix converters.

Modern electrification is impossible without power semiconductors

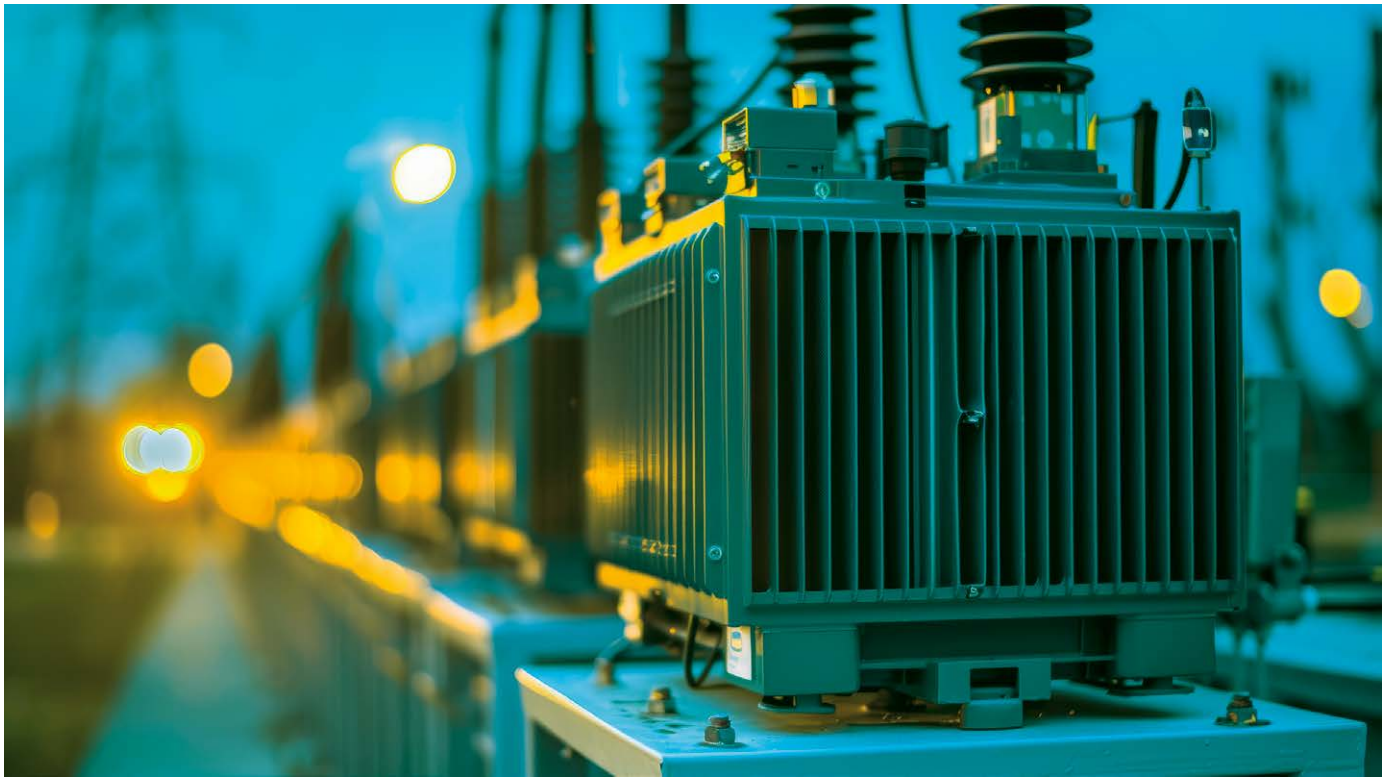
It is clear that power semiconductors have made many applications possible. A large proportion of the world's electrical energy is used to power electric motors, ranging from industrial drives and pumps to compressors and rail systems. It is only thanks to high-performance, fast-switching and precisely controllable semiconductors that the variable speed control we now take for granted is possible, enabling enormous energy savings. Electric mobility in its current form would also be almost inconceivable without modern power semiconductors. Traction inverters, on-board chargers, DC/DC converters and fast-charging infrastructure all rely on these technologies.

In addition, inverters are essential for renewable energies, making energy from photovoltaic or wind power plants suitable for the grid. They are also vital for Data centers, whose highly efficient power supplies would be impossible to realize without modern power electronics.

The new GaN switches and excellent FP (field-plate) low-voltage MOSTFETs provide a solid foundation for the vast field of robotics, improving the performance and capability of everything from humanoid to industrial robots.

The complete electrification of vehicles featuring up to 150 ECUs (Electronic Control Units) has also been realized through the development of specialized power semiconductors, ranging from smart power components for lighting, pumps, and comfort and safety functions, to complex high-voltage drive modules.

Power semiconductors are thus much more than just a component class. They are among the key enabling technologies of modern electrification. st



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Inside the Solid State Transformers

The Solid State Transformer (SST) has been gaining tremendous attention, both in academia and industry, promising extraordinary (often hyped) power conversion performances, well beyond the current state of the art converters. Despite well-evidenced efforts, SST as a technology is still somewhat struggling to gain commercial traction and find its place on the market.

By Prof. Drazen Dujic, Power Electronics Laboratory, EPFL

Rather than reviewing and summarising what has been done already and widely reported by many, this article takes a holistic approach. It presents various technical challenges encountered during the practical design of the SST, which require the attention of the power electronics community and warrant significant research efforts. Addressing and overcoming these technical hurdles will enable SST to become a competitive technology on the market and live up to its promises.

An Emerging Conversion Technology

Now and then, a technology undergoes an (r) evolution, upgrading or significantly improving its performance and ultimately replacing the previously used technology, making it obsolete. The Solid State Transformer (SST), as a new and emerging power electronic conversion technology, is aiming to achieve the same power conversion in various AC or DC power systems, industrial, data centres, and e-mobility infrastructure applications. Numerous demonstrators and prototypes have been presented over the last twenty years or more, yet without a significant commercial breakthrough, which would establish the SST on the market as the primary power electronic conversion technology of choice.

Like many other new technologies, there are techno-economic implications or barriers to reach the relevant market segments, but there are also performance-related metrics that must be sufficient and reliable, offering performance beyond the state of the art, for the new conversion technology to be accepted. This article will focus on the latter, as these can be objectively evaluated and discussed. The objective is not to provide an overview of reported works on the SST, but rather to elaborate on many technological nuances associated with the SST technology as a whole, which are often overlooked, especially in research works originating from academia, and in reality require a great deal of research and engineering attention as implications for the SST technology as a whole are profound.

What are Solid State Transformers?

To discuss and analyse the SST technology, it is important to define it clearly on a system level. It is also important to stress clearly what the SST is not. It is not a direct replacement for a line frequency transformer alone, and it should not be directly compared to it, even though it can obviously perform the AC-AC conversion. The word transformer inside the SST name leads to a lot of confusion,

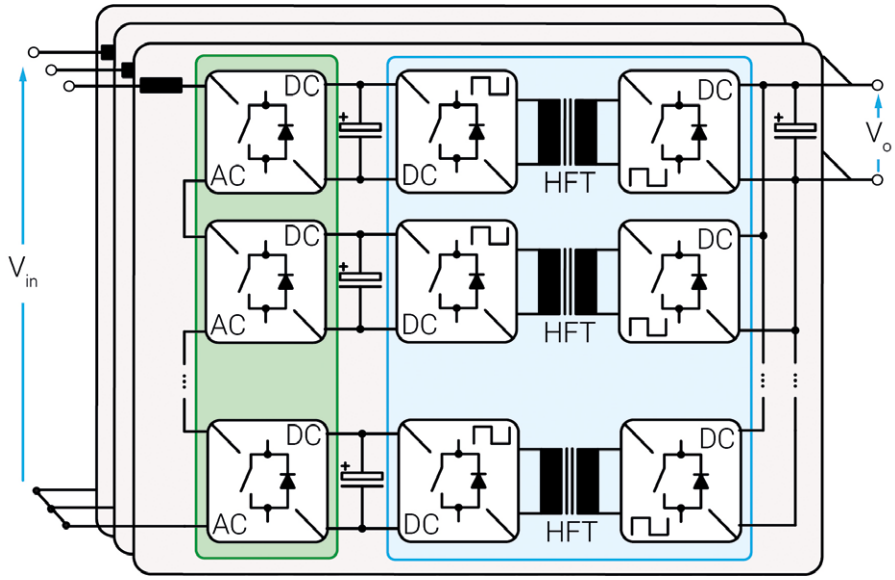

Figure 1: Overly simplified representation of a three-phase SST for MVAC to LVDC conversion, utilizing AC-DC and DC-DC power stages. Identical per-phase arrangements are used and connected in a star connection with a floating neutral point at one end.

unfortunately. Despite various topological variations that exist, the SST is essentially a galvanically isolated modular converter. It has power electronic conversion stages at its terminals, regardless of their number (two or more) and type (AC or DC), and the galvanic isolation is achieved with a plurality of integrated high-frequency transformers (HFTs), operated at several tens or hundreds of kHz. Typically, the SST is a highly modular converter made from many low-power-rated building blocks or modules. It can be designed to perform any conversion: AC-DC, DC-AC, AC-AC, DC-DC, with multiple terminals and with arbitrary numbers of AC phases, even though the single-phase and three-phase AC networks are of practical relevance.

Generally, SST is considered for direct connection to medium voltage networks, serving high power applications in the MW range. It offers voltage adaptation between its terminals, full controllability, and galvanic isolation, needed for safety. While in theory, there is no real limit in terms of applications that SST could serve, some applications (those requiring galvanic isolation) have emerged as early adopters. The fact that SST utilises isolated high-frequency operated DC-DC stages offers the possibility to improve the power density of the SST, both in terms of volumetric (kW/l) and gravimetric (kW/kg) figures of merit. Hence, the applications that would greatly benefit from the reduced form factor of the conversion solution are the main drivers, such as railway on-board power supply, electric vehicle chargers, data centre power supply, etc. Common to these applications is that they require large powers, typically well over 1 MW, are connected to the medium voltage (MV) AC grid, and need to deliver a low voltage (LV) DC supply. Hence, the most popular and studied SST architecture is for the MVAC to LVDC conversion, utilising the input-series output-parallel (ISOP) structure, and will also be used in this article, for the simplicity and clarity of the discussions, as illustrated in Fig.1.

SST Architecture

Many SST architectures have been reported in the literature, and on a system-level, Fig. 2 summarises the generic structure of the main SST module, composed of either two (Fig. 2a) or three (Fig. 2b) cascaded power stages performing:

- AC-DC or DC-DC non-isolated power conversion
- DC-DC (AC-AC) isolated power conversion
- DC-AC or DC-DC non-isolated power conversion

The exact power electronics topologies inside each of these modules are not fundamentally relevant for the objectives of the article. Not all stages are always needed, and many proposed SSTs are based only on the two-stage architecture, combining one isolated and one non-isolated stage. Finally, a single-stage solution, utilising only isolated stages performing DC-DC or AC-DC conversion, is also possible, but not further discussed.

Furthermore, these modules are connected either in series or in parallel, on either of their sides, to increase the voltage and/or current ratings in accordance with the application needs. Irrespective of the nature of the application system on either side (AC or DC), all four combinations typically used in power electronics, to increase the voltage and/or current ratings, are utilised, leading to the emergence of modular structures as shown in Fig. 3:

- ISOP: input-series, output-parallel
- ISOS: input-series, output-series
- IPOP: input-parallel, output-parallel
- IPOS: input-parallel, output-series

In pure DC applications (e.g., DC-DC SST) or a conversion in a single-phase AC system (e.g., AC-DC SST), resulting modular structures are sufficient. Three-phase applications typically combine these single-phase structures in a star/delta connection on their AC side, as already hinted in Fig.1. In summary, the SST is a highly modular, galvanically isolated, power electronics converter, which can be realised in an infinite number of ways, by simply choosing different power electronics topologies inside the power stages. Being modular implies that it is also scalable in terms of voltage and current and can be arranged for the needed application ratings. Being isolated, thanks to the presence of isolated DC-DC stages, implies a design degree of freedom in choosing

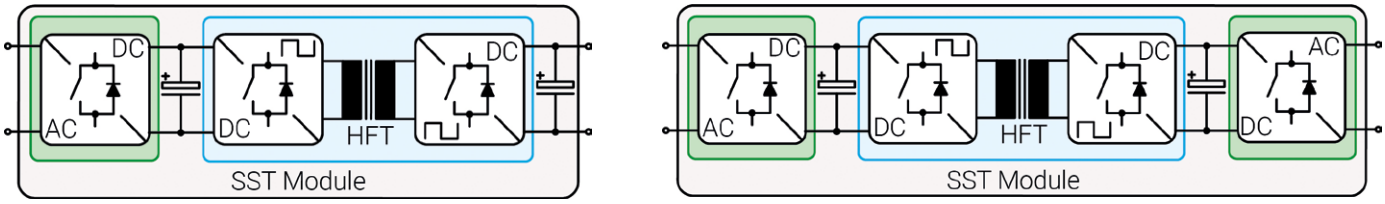

Figure 2: The generic SST module is typically composed of: a) two cascaded power stages for the MVAC to LVDC conversion as illustrated in Fig.1; b) three cascaded power stages for the MVAC to LVAC conversion.

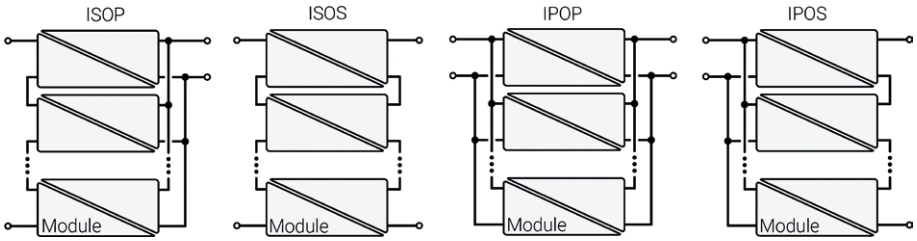

Figure 3: Common arrangements of the basic modules inside the SST.

the operating frequency and technologies for the HFTs. Yet these basic features also translate into many challenges in the real world, and are subject to many design trade-offs, as discussed shortly.

SST Technology Challenges

Despite numerous promises and prototypes, realising an SST and launching it as a successful commercial product on the market has proven challenging so far. There are several technical reasons for this, which are related to the internal architecture of SST, requiring a careful engineering design approach and, in some cases, even further research efforts. Realising the MV-rated converter, with the limited blocking voltages of available semiconductor devices, naturally leads to modular SST designs. Each module contains one or more power electronics stages, mechanically enclosed, electrically and thermally managed, with various signal level electronics (gate drivers, sensors, local controllers), auxiliary power supply (internal or external), communication interfaces with adequate isolation capabilities, including an HFT, as well. There are many interfaces to be managed on the SST module level: electrical (power), thermal (cooling), mechanical (integration), communication (signal), auxiliary power (if external). Even if a single SST module is of modest complexity, many of them need to be mechanically arranged, interfaced, and precisely time-coordinated during normal operation and under fault conditions.

Modularity and Scalability

In a modular SST design, each module is designed to have the specific power, voltage, and current ratings derived and determined somehow. For the sake of illustration and ease of discussion, let's assume that a single SST module is rated for 100kW, operates with a 1.5kV internal DC link, and can output on the AC side voltage with ±1kV peaks or AC RMS voltage up to 1kV, while it provides 800V on the DC side (data centre requirement nowadays). In addition, the HFT inside the module is designed with specific isolation capabilities, considering the highest MVAC voltage that must be withstood during operation. Let's assume that a 100kW HFT is isolated to safely operate with MVAC grid voltages up to 10kV±10% (line-to-line voltage). Having well-defined module ratings directly impacts the SST scalability, making it possible to achieve only a certain system level rating easily. This is generically illustrated in Fig.4 by considering AC-DC ISOP SST and several possible system ratings, as discussed later. If the SST module has well-defined ratings, the series connection of modules increases voltage handling capabilities on the AC side, and the addition of every module increases the overall power ratings of the SST. However, the isolation capabilities of the HFTs are ultimately defining the maximum MVAC utility voltage that can be reached. In the presented example and considering grid voltage variations and control needs, at least 6 modules per phase of SST are needed for operation from a 10kV AC grid, resulting in an SST design with 18 modules in total or an overall power of 1.8MW.

In case SST should be operated in a higher voltage grid, for example 36kV±10%, new HFTs with higher isolation capabilities are required and must be designed. Let's assume 100kW HFTs are redesigned for working voltage of 36kV and all other existing parts can be reused, since insulation problem of cascading power stages is solved anyhow outside the power stages. Now at least 23 modules per phase of SST are needed or 69 modules in total to connect to 36kV utility grid, yielding overall power ratings of 6.9MW.

This is illustrated, somewhat simplified, in Fig.4. There exists an available SST design (AD) that can connect to some AC grid voltage, and deliver some power (both are normalised), and this can be achieved thanks to the available HFT1 design inside the DC-DC power stages and the connection of a certain number of SST modules, as discussed earlier. If the SST power ratings need to be increased, irrespective of the utility grid voltage, this is only possible by paralleling the available SST modules, or complete SSTs, which effectively means that power can only be doubled, tripled, etc., and only a limited number of power ratings can be achieved. This is illustrated by sloped lines, representing SST scalability due to different current ratings of the available SST modules, e.g. i or 2i or 3i.

Hence, operating point 1 (OP1) is achievable, eventually by paralleling SSTs. In case that the technical requirement is to achieve OP2, that is not possible with HFT1 due to its isolation capabilities and a new design with higher isolation capabilities is needed, HFT2, to allow cascading more of the SST modules to reach higher MVAC voltages. Still, in case that OP3 is needed in an application, the solution is not obvious, other than to offer a slightly oversized solution in terms of power (above OP3 at the intersection with the 2i sloped line). Alternatively, a completely new SST module design is likely needed, having different voltage and current ratings to be cost-effective. Certain application requirements, such as low-voltage with high-power ratings (OP4) or high-voltage with low-power ratings (OP5), would require module design to consider them from an early stage, if techno-economically feasible at all.

This scalability problem is not unique to SST

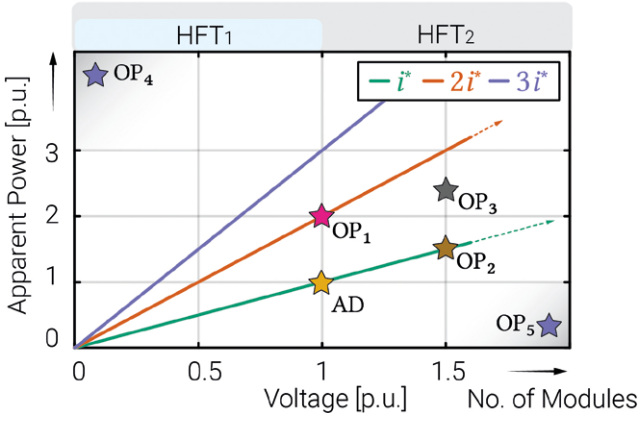

Figure 4: Scalability challenges of the SST that need to be addressed from an early design phase, based on the desired coverage of the market (application) in terms of power and voltage ratings.

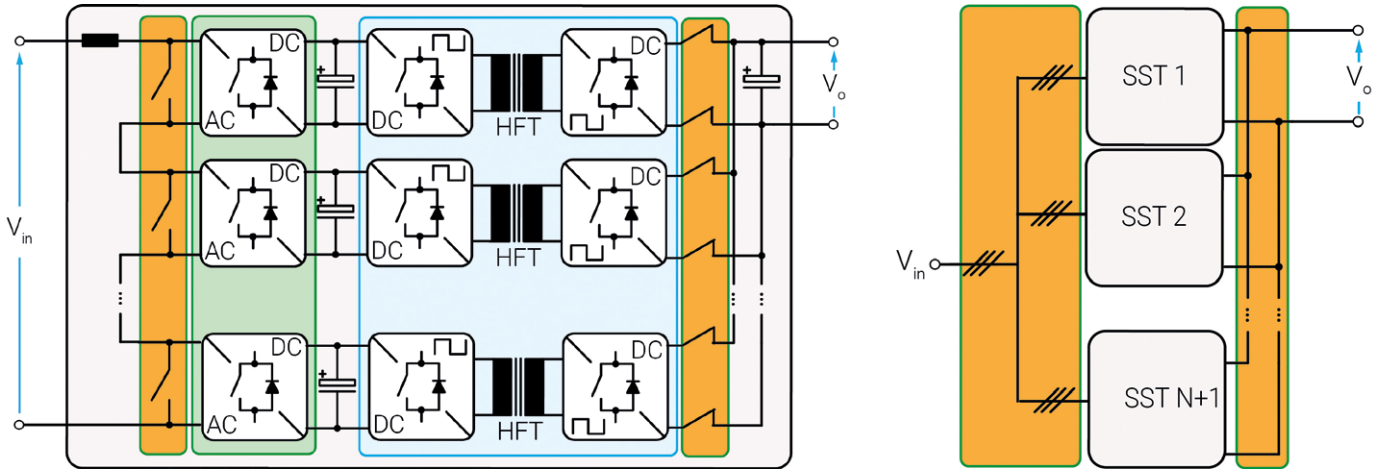

Figure 5: SST redundancy dilemma: a) SST with per module implemented redundancy allowing for the isolation of the faulty module on both AC and DC sides; b) Multiple SST without any internal redundancy, operating in parallel, and having redundancy implemented on the system level.

and can be found in many other modular converter designs. Yet, the key difference is that SST modules integrate HFTs, which need to be custom-designed, with sufficient isolation capabilities, and are not commodity products, as semiconductor devices, available in standardised voltage classes.

Reliability, Availability, Redundancy

Modularity as a design feature does provide advantages and benefits in the production, due to the volume of scale, opportunity to use lower voltage-rated devices, but also introduces many possible points of failure in the actual SST design. Modularity, if properly executed, concentrates the limited fault energy in a well-contained space, typically around the DC link of the module, but also requires subsequent isolation of the faulty module from the rest of the system, if SST is supposed to continue to operate afterwards, upon successful isolation of the internal fault.

A high number of SST modules equipped with power semiconductors, gate drivers, sensors, capacitors, inductors, auxiliary electronic circuits, etc., results in challenges to ensure high reliability indices. Furthermore, the lack of statistical field data and user experience is not available for SSTs now, to feed back valuable information into new designs. Nevertheless, high up-time or availability must be ensured, and this is addressed typically by implementing some sort of redundancy into the SST design by means of the addition of one or more extra SST modules in series, increasing their overall number beyond the bare minimum for the correct operation. Using the previous example, let's assume that a previously designed SST with 18 submodules for a 10kV grid is equipped with an extra SST module per phase. The SST with implemented redundancy now has 7 SST modules per phase or 21 in total.

Implementing redundancy inside the SST brings new design challenges, as for a redundancy to work, all SST modules must be equipped with means to be bypassed and isolated from the rest of the SST in case any of them is faulty. This bypass equipment must be present on both SST module terminals and must act fast and reliably. It increases the module but also the whole SST complexity, cost, size, and it needs control resources and eventually auxiliary power for its operation, as illustrated in Fig.5a. For an ISOP SST, a solution for achieving a short-circuit is needed on the AC side, and a solution for achieving an open-circuit on the DC side, to completely isolate a faulty module.

Whether the redundancy is needed inside the SST or not will greatly depend on the application or the imposed technical requirements. If one assumes that many SSTs will be installed in parallel to provide power to a facility of some sort, then implementing N+1 or N+2 redundancy on the system level is likely more cost-effective (Fig.5b). Some applications may even require a complete redundant 2N system with many SSTs without any internal redundancy. On the other hand, a single SST designed for a specific application and installed as a single unit may require redundancy to be implemented internally, on a per-module basis (Fig.5a).

High Frequency Transformers

For many years, low-voltage switched mode power supplies have greatly improved their power density thanks to high-frequency operated power semiconductors and low-loss, high-frequency, magnetic materials, enabling reduction of HFTs inside. In a way, the SST aims to achieve the same for the high voltage multi-MW conversion.

One of the key features distinguishing SST technologies is the presence of the high-power HFTs, providing galvanic isolation and voltage adaptation inside the SST DC-DC module. Even if voltages applied to the winding of these HFTs are small (e.g. ±1500 or ±800V), the isolation design between windings must be carried out considering AC grid working voltages and suitable standards for the insulation coordination to ensure safety in operation. This is proving to be challenging for several reasons. The expectations to greatly reduce the size of HFT by simply increasing its operating frequency are quickly challenged by isolation distances needed to ensure safety – hence further increasing the switching frequency only increases the losses and impairs the SST efficiency. There are numerous insulating materials available and applicable for HFT designs, but the power electronics community has certain reservations towards some or generally not sufficient knowledge in this domain. Isolation designs of HFT relying on air are simply too bulky to be attractive, while oil or other isolating liquids are often not desired, despite having an excellent track record in distribution transformer designs. The solid insulation design is often pursued as a highly attractive approach, despite manufacturing challenges and uncertainties associated with long-term operation of dielectrics under mixed-frequency stresses, thermal stresses, partial discharges, and potentially catastrophic failure of winding insulation. The HFT technology for the SST is often largely

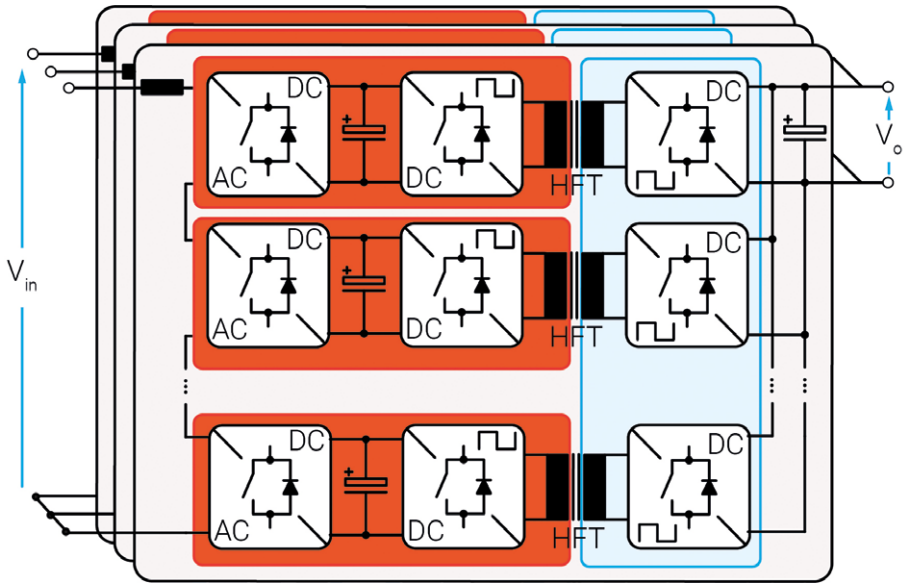

Figure 6: The cost of isolation inside the SST: there is a trade-off between ensuring safety in design and achievable power density on the system level.

underestimated, despite having a very large impact on the overall SST performance. This is an area of active research nowadays.

Insulation Coordination and Power Density

It should be already obvious that SST is a medium voltage converter and must be designed in accordance with well-established safety design guidelines, summarised in various insulation coordination standards. In addition to HFTs' isolation, the selection of types of isolation levels and insulating materials must be carried out and applied to a complete SST, considering relevant over-voltage categories, pollution degrees and other deciding factors. Isolation distances between the SST modules, modules and the SST enclosure, must ensure safety of equipment and personnel during operation.

With a high number of SST modules and considering MVAC grid voltages (e.g. 36kV), a significant space or volume must be dedicated to the isolation, which can significantly impact and increase the overall volume and reduce the power density of the SST during practical realisation, as shown in Fig.6. For an ISOP SST, AC-DC stages and part of DC-DC stages are all floating and need to be isolated for a full working voltage against the SST enclosure and surrounding. As already discussed, complete system working voltage also appears across the windings of each of the HFTs. It can be increasingly noticed that almost none of the companies working on the SST use power density metrics to describe system-level performances, which used to be the main selling point and all are rather pitching the high efficiency nowadays. Nevertheless, this is a matter of practical engineering design, and careful selection of materials during insulation coordination.

Control Hardware and Software

On purpose, this article does not discuss power electronics topologies or power semiconductors inside the SST modules, as these are simply a design choice that can be motivated by many factors coming from a system-level design perspective such as efficiency, cost, desired number of modules, etc. The control objectives of an SST performing MVAC to LVDC conversion are generally easy to explain and achieve, as these are identical with those of other converters: AC grid current control and DC output voltage control, with various internal control objectives depending on the used topologies for power stages of SST modules.

The challenges emerge due to the high modularity of the SST, where many modules must be coordinated to operate in a synchronised fashion supporting the overall control objectives. Hence, control hardware architecture must be distributed (as well as control software), and some kind of hierarchical levels must be established. At the level of the SST module, one may have one control card managing the complete module, but there could also be control cards allocated to each power stage of the SST module. Outside the single SST module, many of them in series connection of one phase may be supervised by another control card managing the complete SST phase (if available) or directly from the central control card managing all SST modules at once. Clearly, there is no single way to achieve this, and many control hardware layouts are possible.

As the number of SST modules can greatly vary inside the SST, control hardware must be able to accommodate various topological configurations, exchange relevant data between various control cards, control commands and references, state machines at different levels, coordinate and synchronise the pulse width modulators, manage sensors, faults, coordinate the protection coordination, etc.

While not strictly relevant for the SST control, the control cards, gate drivers, sensors, and all electronics inside the SST module require certain auxiliary power to operate. This can be provided locally from the energy stored in DC link capacitors, provided these are charged somehow, either from the AC grid or by an external pre-charge solution, prior to SST commencing its operation. Alternatively, low-rated auxiliary power may be provided externally, not needing SST to be energised, requiring high-voltage isolated external power supplies, isolated for the same working voltage as the complete SST. Realising these solutions is another active area of research.

Efficiency

The SST efficiency is not a random outcome of the design, but a requirement that will be increasingly imposed by the applications and customers, as SST technology gets accepted. As mentioned in the introduction, many SST designs use multiple cascaded power stages inside the SST module. As every SST module processes a fraction of SST power, its efficiency is a good indicator of the overall SST efficiency. If we assume that each power stage has 99% efficiency, then an SST module having internally two cascaded stages (e.g. AC-DC + DC-DC) would have an efficiency of 98.01%, while the module with three stages (e.g. AC-DC + DC-DC + DC-AC) would offer an efficiency of 97.03%. Connecting many modules to arrange the final SST, and considering other elements of losses outside the modules, these numbers will drop further, likely by another 0.5% to 1%.

On the other hand, looking into the efficiency numbers announced by companies working on the SST technologies, targets are set to 98.5% and above, for the complete SST. Re-

peating previous calculations and assuming now that each power stage has 99.5% efficiency, yields an SST module efficiency of 99% for a two-stage solution and 98.5% for a three-stage solution, without considering other sources of losses inside the SST.

Achieving these operational efficiencies is a matter of the overall SST design optimisation, choice of power electronics topologies, power semiconductors, switching frequencies, magnetic devices and selected modulation and control principles. There are numerous ways to achieve them, and the power electronics community will only get better at doing so, as competitive SST solutions reach the market and relevant applications.

Summary

Even though this article is technology-motivated, it is not easy to delve into all nuances associated with practical power electronics design of the SST. The wording SST technology is deliberately used, as there is no consensus in the power electronics community on what is and should be inside an actual SST. The author's opinion is that SST is a galvanically isolated modular converter, combining various technologies inside and with endless optimisation opportunities and topological variations. As the technical requirement specifications get clearer for various applications, it will be possible to design and optimise SST technology, specifically tailored for the application needs, making it a cost-effective solution providing expected performances.

Perhaps the best way to close this article is to jump into the future and apply an approach from the industrial product management and consider the SST as the product from the user perspective. The Features, Advantages, Benefits (FAB) approach or the framework helps businesses communicate product value to the end users (customers). Features are factual descriptions of the SST characteristics, something that typically excites the researchers and engineers the most. Advantages describe how these features are beneficial for the SST as an advanced conversion system, and hence SST manufacturers are interested in implementing useful features. Benefits explain the positive outcomes that the end-user experiences in an actual application where the SST is used, because of the utilised features implemented by the SST manufacturer. A rather trivial example would be that any converter with a multilevel voltage waveform (Feature) requires less passive filtering and hence needs a smaller filter (Advantage), resulting in a smaller footprint of a final converter (Benefit). Yet, most of the time, the end-user or the customer may not care or even understand many internal features of the SST. While numerous benefits are claimed for the SST, especially in the academic literature, one needs to approach the analysis carefully and separate technical jargon and hype from the actual engineering reality and deliver and ensure performance indicators that are measurable in the real world. Meanwhile, all the major companies, as well as newly created start-ups, are working on this. So it's an exciting time, and the SST technology is great — it's coming now!

Publishing Details
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ADVERTISING
Mesago Messe Frankfurt GmbH
Phone +49 711 61946-144
fabian.brenner@mesago.com

EDITED BY
Engelbert Hopf (eg),
Iris Stroh (st),
Markt&Technik, Componeers GmbH

DESIGN
Wolfgang Bachmaier,
Alexander Zach,
Componeers GmbH

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